VHDL Implementation of Sigma-delta Beamformers for Ultrasound Application

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Abstract: This paper presents the VHDL implementat1ion and the evaluation, in terms of hardware and power consumption, for 3 different sigma-delta beamforming (SDBF) algorithms. Synthesis was done at 160MHz operating frequency using Synopsys Design Vision with 0.18µm process. By taking the pre-delay reconstruction SBDF algorithm as reference, the post-delay reconstruction SDBF consumes only 10.71% of total dynamic power and 6.49% of total area. On the other hand, the post-delay reconstruction algorithm with insert-0 artifact correction technique consumes 11.68% of total dynamic power and 6.90% of total area.

1. Introduction

Sigma-delta beamformer (SDBF) has been proposed as a potential single chip solution for ultrasound beamforming system. It replaces the multi-bit ADCs in the conventional multi-bit digital beamformer with sigma-delta ADCs (including the modulators and reconstruction filters). This is known as the pre-delay reconstruction SDBF which achieves good image quality just as its multi-bit counterpart. However, due to the design that one reconstruction filter for each channel, it has the limitation of number of channels in the system. If the number is large, the power and hardware consumptions would be very high.

In order to minimize the hardware, Noujaim *et al.* proposed a post-delay reconstruction SDBF (or called repeat-sample method) which utilizes only one reconstruction filter in the entire beamformer [1]. However, it suffers from dynamic focusing artifact problem which degrades the output image quality. The artifact problem is due to the amplitude distortion of signal reconstructed by the reconstruction filter. By applying the post-reconstruction algorithm, the samples are selected according to the delay profile. The delay profile was updated at every clocking instance of the system clock. However, due to the quantization of calculated profile, there would be cases that particular samples are selected twice in adjacent clock period. Since Delta-sigma analog-to-digital conversion is a kind of Pulse Width Modulation (PWM), in order for further process, the reconstruction filter is designed to convert PWM signal into Pulse Code Modulation (PCM). The PCM output depends on a group of adjacent samples instead of a single sample. Therefore, this sample repetition could cause the distortion. Since in pre-delay reconstruction SDBF, the reconstruction is done before the samples are selected, the sample selection has no effect on the reconstruction. Hence, the pre-delay reconstruction SDBF is free of artifact problem.

Hence, Freeman *et al.* proposed an insert-0 method [2]. The insert-0 method allows the system to detect sample repetition by tracking the delay profile applied, and replaces the repeated sample with a zero in order not to generate distortion, hence corrects the artifact problem.

The aim of this paper is to evaluate the feasibility of implementing these algorithms onto a single chip, thereby to facilitate a low-cost hand-held ultrasound device.

2. Design and Implementation

The beamformer implemented includes all sub blocks used after sigma-delta modulator until the output of the reconstructed beam-summation.

2. 1 System Design Specification

The design specifications are listed in the Table 1.

Table 1. System design specifications.

No. of channels	64
No. of memory cells per channel	144
System operating frequency	160MHz
Output frequency	20MHz

The input and output configuration for 3 different beamformers were designed to be same. In total, there're 6 input signals for a beamformer. The system clock signal, the asynchronous reset signal, as well as an input command signal and an output command signal are the 4 control inputs to the entire beamformer. The 2 command signals were designed to provide external control ability when the beamformer works as a sub-module in the ultrasound system. Besides, for every beamforming channel, there are a processing data input, which is the output of sigma-delta modulator (1-bit) and a reference data input, which is the calculated delay profile for the corresponding channel (8-bit), that is, 64-bit processing data input and 512-bit reference data input in total, as shown in Fig. 1 below.

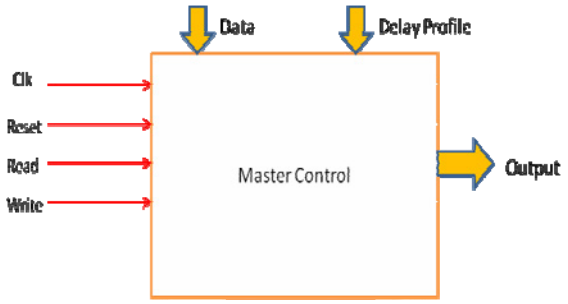

Fig. 1. System I/O configuration for 3 beamformers.

2. 2 Pre-delay reconstruction SDBF

The pre-delay reconstruction SDBF, which was used as a reference, was implemented with 64 pre-reconstruction filter components, one for each channel, as shown in Fig. 2. One filter component was built as a 161-stage FIR filter. The filtered data are stored in memory components, which were designed as an 8-bit shift register with 144 cells. The samples stored are selected according to the delay profile inputted and then summations are performed by a set of 2's compliment adders. Due to the specification that the output frequency is 1/8 of system operating frequency, the signal is decimated 8 times during the beam-summation by controlling the working frequency of the adders. A clock divider was used to generate the clock signal for adders from the system clock.

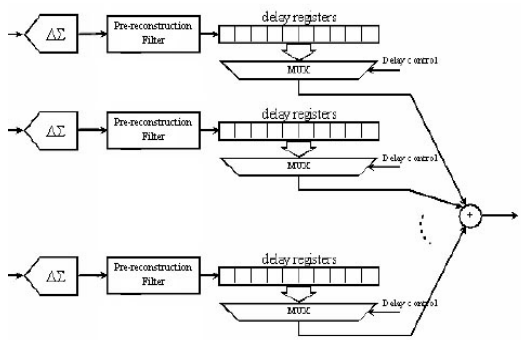

Fig. 2. Pre-delay reconstruction SDBF structure.

2. 3 Repeat-sample method

The repeat-sample method was implemented closely following the design of basic post-delay reconstruction architecture, with a top-level entity, a memory component, a set of adders and a set of decimation filters, as shown in Fig. 3. The memory component was designed as a single-bit shift register with 144 cells. The decimation filter set consists of a 3rd order CIC decimation filter with decimation factor of 8, as well as an FIR filter for noise reduction. The adders were designed as simple binary adders. In addition, a converter is also included to convert the input of decimation filter from unsigned binary value into signed value in 2's compliment representation, which is required by the filter design.

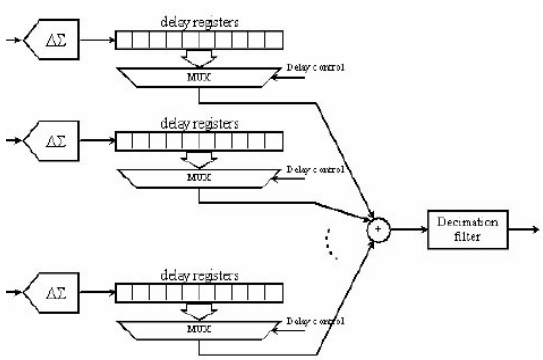

Fig. 3. Post-delay reconstruction SDBF structure.

2. 4 Insert-0 method

The insert-0 method was implemented by introducing one extra block to the conventional post-reconstruction architecture, of which is to detect the artifact from occurring by tracking the delay profile applied, and to correct the distortion by replacing the repeated samples by 0. This block was designed that one block for each channel, following the memory component. Data flows through this block before summed by the adders. Besides the distortion correction, this block performs the same function as the converter applied in the repeat-sample architecture if no repetition detected. Hence, the adders were designed as 2's compliment adders, instead of simple binary adders that used in the conventional post-reconstruction architecture.

3. Evaluation Results

The evaluation of the beamformers was done in terms of the relative image quality, the power consumption and hardware complexity, which are the essential aspects determine the functional performance and the feasibility to be implemented on a singer chip.

3. 1 Image quality

The image quality comparison was done through the simulation of the center scanline of a synthesized point phantom image with 10 wire targets. Desired output sample set was also provided for functional correctness checking.

Fig. 4 shows the simulation result for pre-delay reconstruction SDBF, which was used as the reference for the image quality evaluation. Intuitively, the pre-delay reconstruction SDBF is able to generate the most sharp and clear image than the other two SDBF, since it is totally free of artifact problem. the Because the artifacts are amplitude distortion of the output signals, the distribution of artifacts for the repeat-sample method and the effectiveness of artifact-correction for the insert-0 method could be directly seen by compare the simulation result of the 2 beamformers with the reference.

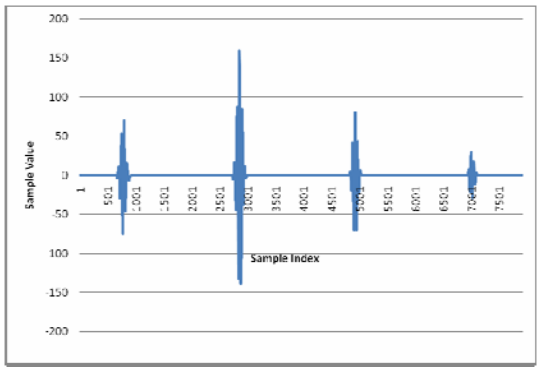

Fig. 4. Simulation result for Pre-delay reconstruction SDBF

The difference of 3 beamformers in terms of image quality can be deduced from Fig. 5., which plotted the absolute difference for repeat-sample output values from pre-delay reconstruction ones, as well as difference for insert-0 output values from pre-delay reconstruction ones,

in order to directly reflect the distortion introduced by the sample repetition As shown in Fig. 5, using pre-delay reconstruction output as reference, i.e. 0s for all sample index in Fig. 5, the repeat-sample output consists of artifacts from near field to the far field. Within the peak intervals, the artifacts are more obvious due to the relatively higher distortion. The insert-0 method was able to reduce the artifacts effectively. As shown in lower part of Fig. 5, most of the distortions are removed, except for those relatively highly distorted intervals, that is, the intervals around the peaks. This implies that on the final image, the insert-0 method effectively cancels the artifacts all over the background, but would have certain amount of artifacts shown around the target image.

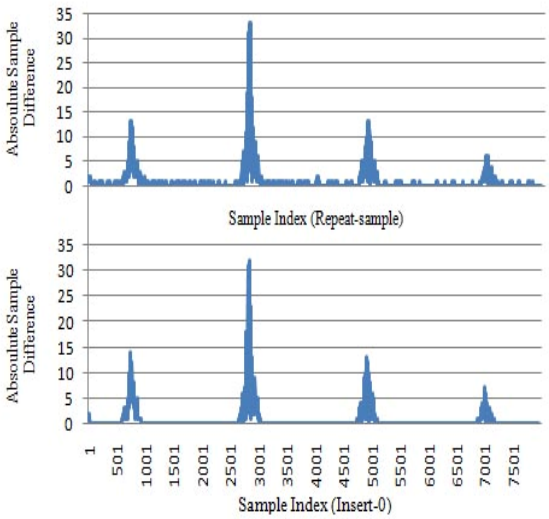

Fig. 5. Image quality comparison.

3. 2 Power consumption

The power and hardware performance comparison was done through the results of synthesis by using Synopsys Design Vision, version X-2005.9-SP2, with 0.18μm process.

For the power consumption, according to Table 2 and Fig. 6, taking pre-delay reconstruction result as reference, the total dynamic power consumption of repeat-sample is 10.71%, which is equivalent to 90% reduction, whereas the consumption for insert-0 algorithm is 11.68% of the amount consumed by pre-delay reconstruction algorithm.

The high power consumption for pre-delay reconstruction is due to the high-speed pipeline processing and large amount of arithmetic operation for all pre-reconstruction filters. Since the one filter is required for every channel, for system with large number of channels, for example, 256 channels, the insert-0 method SDBF would have obvious advantages over the pre-delay reconstruction SDBF, in terms of power consumption.

Table. 2. Synthesis results for power consumption.

	Pre-recon	RS	Ins-0
Total Dynamic Power (mW)	2793.70	299.34 (10.71%)	326.20 (11.68%)

(RS ≡ Repeat-sample; Ins-0 ≡ insert-0; Pre-recon ≡ pre-delay reconstruction, which is the reference)

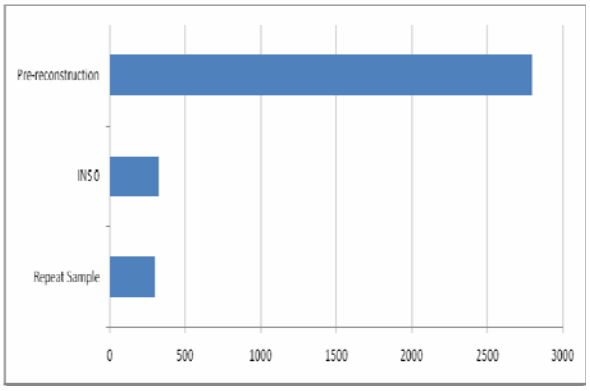

Fig. 6. Power consumption comparison.

3. 3 Hardware complexity

As for hardware complexity, according to Table 3 and Fig. 7, taking the pre-delay reconstruction algorithm as reference, the repeat-sample method reduced more than 90% of the hardware consumption, which is only 6.49% of the total area utilized by pre-delay reconstruction algorithm in terms of total area. The insert-0 algorithm consumed slightly more, which is 6.90%, due to the extra artifact correction component.

The significant high hardware complexity of pre-delay reconstruction algorithm is due to the computationally demanding pre-reconstruction filters, since there are multiple filters used in the system. Similarly as the power consumption, the insert-0 method SDBF would have more obvious advantages over the pre-delay reconstruction SDBF, in terms of hardware complexity, as the number of channel within the system increases.

Table 33. Synthesis results for hardware complexity.

	Pre-recon	RS	Ins-0
Total area:	2292982.25	148769.42 (6.49%)	158282.36 (6.90%)

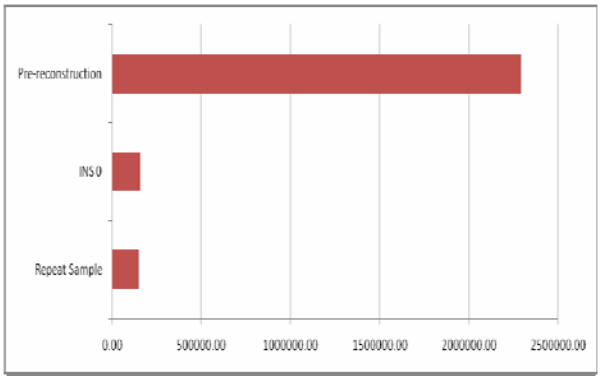

Fig. 7. Hardware complexity comparison.

4. Conclusion

At 160MHz operating frequency, the post-delay reconstruction SDBF consumes only 6.49% of total area and 10.71% of total dynamic power, by taking the pre-delay reconstruction SDBF as reference. On the other hand, the post-delay reconstruction algorithm with insert-0 artifact correction technique consumes slightly higher hardware and power (6.90% of total area and 11.68% of total dynamic power consumed by pre-delay reconstruction SDBF) but preserves the image quality as the pre-delay reconstruction SBDF algorithm.

References

[1] S. E. Noujaim, S. L. Garverick, and M. O'Donnell, "Phased array ultrasonic beam forming using oversampled A/D converters," U. S. Patent 5203335, April 20, 1993.

[2] S. R. Freeman, M. K. Quick, M. A. Morin, R. C. Anderson, C. S. Desilets, T. E. Linnenbrink, and M. O'Donnell, "Delta-sigma oversampled ultrasound beamformer with dynamic delays," *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 46, no. 2, pp. 320-332, March 1999.