Current Testable Design of Resistor String DACs for Open Defects

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Abstract: In this paper, a DFT method of resistor string digital-to-analog converters (DACs) is proposed so as to be tested fully by supply current testing. Targeted defects are opens in the DACs. Testability of opens in testable designed DACs is examined experimentally. The results show that all of the opens in an N-bits testable designed DAC will be detected with test vectors of about 2(N-1) by supply current testing.

1.Introduction

DACs are core elements in mixed signal ICs. Many DACs have been used to implement analog-to-digital converters(ADCs) and tested as a part of ADC tests.

Until now, many kinds of ADC test methods have been proposed[1,2]. Also, various kinds of DFT(design for testability) methods and BIST(built-in self test) ones for ADCs have been proposed[3-8]. For example, an ADC and a DAC in an IC are tested simultaneously by connecting the output terminal of the DAC to the input one of the ADC. By providing a digital value to the DAC, the output signal from the DAC is converted with the ADC. By comparing the converted digital value to the input digital one, both the DAC and the ADC are tested simultaneously[4,5]. However, there are many ICs in which only DACs are implemented without ADCs. In the ICs, tests of DACs are indispensable.

Many mixed signal ICs including DACs have been implemented with an SoC technology. Shorts and opens have often occurred in the ICs. However, many DACs have been tested by examining the functionality by a classical test method[2]. It has been difficult to test DACs in the ICs by the test method owing to the low observability of signals. Furthermore, shorts and opens may not be detected with high coverage by the test method.

On the other hand, it has been shown that current testing is useful for detecting shorts in CMOS logic ICs. It is expected that shorts in DACs implemented in an IC are detected easily by current testing like in the tests of CMOS logic ICs. Thus, we have examined testability of shorts and opens in a DAC in order to check the feasibility of DAC testing based on supply current[9].

In the testability analysis, we have selected a resistor string DAC as a targeted one, since resistor string DACs have been used in many ICs. The results suggested us that it was difficult for opens at MOSs in the DAC to be detected by supply current testing. Thus, we have proposed a testable designed DAC so that opens in it could be detected by supply current testing in [9].

However, as the number of bits of a targeted DAC becomes large, all opens may not be detected. Thus, we attempted to develop a new testable design method of DACs so as for all of the opens to be detected by supply current testing.

In this paper, we propose the DFT method. Also, we show testability analysis results of two DACs designed by using our DFT method.

2. Supply Current Testing of Resistor String DACs

Resistor string DACs have been often used in mixed signal ICs. A resistor string DAC is made of a resistor string and MOS switches. Besides them, an operational amplifier and inverter gates are added to the DAC. An example of the DAC is shown in Figure 1. The DAC is a 3 bit one.

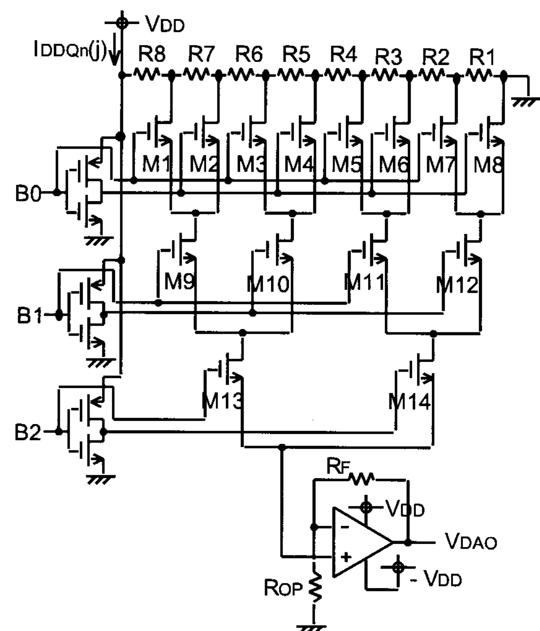

Figure 1. 3 bits resistor string DAC

Each of the MOS transistors in the DAC acts as a switch. By providing logic values to the primary input terminals, nMOSs are turned on whose gate voltage is H level. Output

voltage of the DAC depends on which nMOSs turn on. For example, when B0=B1=B2=H and R_{op}=R_F, the output voltage, V_{DAO}, is defined by Eq.(1).

$$V_{DAO}=(V_{DD}/8R_i)*7R_i \qquad (1)$$

where R_i is the resistance of R_1,•••, R_7 and R_8.

Output voltage of a resistor string DAC depends on input logical vectors. Moreover, in a defect-free N bits DAC, quiescent supply current, I_{DDQn}, flows from V_{DD} to GND, which is defined by (2).

$$I_{DDQn}=V_{DD}/(2^N*R_i) \qquad (2)$$

In our tests, quiescent supply current is measured to detect defects in the DAC to be tested. If Eq.(3) is satisfied for any test vectors, we determine that a defect occurs in the DAC to be tested.

$$| I_{DDQC}(j) - I_{DDQn}(j) | \geq I_{th}(j) \qquad (3)$$

where I_{DDQC}(j) and I_{DDQn}(j) are the quiescent supply current of a DAC under test and the one of defect-free DACs measured in the j-th test vector application, respectively. Also, I_{th}(j) is a threshold value, which is used for determining whether the DAC is faulty, or not. If Eq.(3) is not satisfied for all of the test vectors, we determine that the DAC is defect-free.

Our targeted opens in a DAC are the followings: opens in a resister string, opens at source and drain terminals in an MOS. Opens at gate terminals of MOSs are not targeted, since the defects will generate unexpected behaviors and be detected by conventional test methods.

I_{DDQn}(j) will flow into the defect-free DAC. When a short occurs between terminals of a resistor in the resistor string, larger quiescent supply current will flow than I_{DDQn}(j). Thus, the defect will be detected by Eq.(3).

Also, when a short occurs between a source terminal and a drain one in a MOS, a new current path will appear owing to the short in the circuit. For example, when a short occurs between the drain and the source terminals of M10, a current path, Path#3, will appear as shown in Figure 2 and larger supply current will flow than the defect-free DAC.

When an open occurs in the resistor string, no supply current will flow. Thus, the open will be detected by Eq.(3). On the other hand, even if an open occurs in a MOS switch, the open will not be detected by Eq.(3), since almost zero current flows into the input terminal of the operational amplifier through the MOS switch in the defect-free DACs.

We evaluated feasibility of the current tests experimentally[9]. In order to evaluate it, we had designed a layout of a 3-bit resistor string DAC with ES2 0.6μm CMOS process technology. R_i in the resistor string is 625Ω and V_{DD} is 5V. We had converted the layout into a Spice file and derived I_{DDQn}(i) and I_{DDQC}(i) with PSpice. In our experiments, a short is inserted between targeted terminals by adding a resistor of 0.1Ω between them to the Spice file of the defect-free circuit. An open is inserted to a targeted terminal by adding a resistor of 10 GΩ to the SPICE file. I_{th}(j) of Eq.(3) used in the experiments is 10% of the quiescent supply current of the defect-free DAC for the j-th test vector application, I_{DDQn}(j).

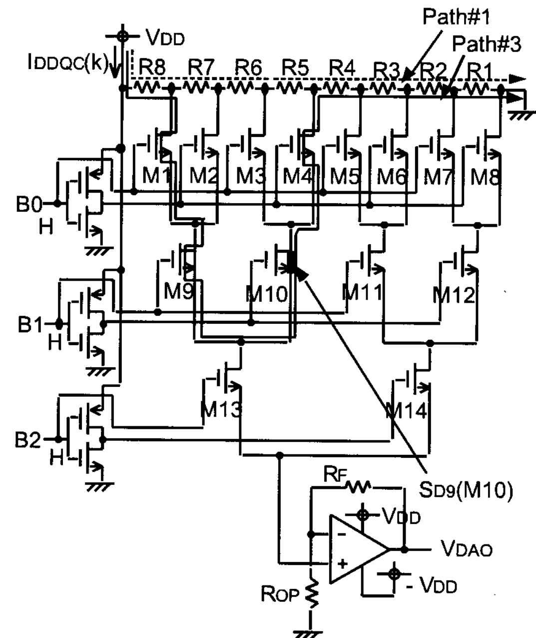

Figure 2. Additional supply current path caused by a short in M10

It had been shown by our experiments that all of the shorts would be able to be detected by current testing based on Eq.(3)[9]. However, no opens in the MOS switches had been detected, since almost zero current flows into the input terminal of the operational amplifier. Thus, we attempted to develop a current test method for detecting opens in a resistor string DAC.

3. DFT of DACs for Current Testing

Opens in MOS switches may not be detected by the current testing based on Eq.(3). It stems that almost zero current will flow through the MOS switches in defect-free DACs and faulty DACs having opens. In order to detect opens in MOS switches of DACs by current testing, we attempted to develop a DFT method for resistor string DACs. A DAC designed by using our DFT method is shown in Figure 3.

In our design, a circuit consisting of an inverter and an OR gates is added to each input line. Furthermore, an nMOS, M_g, is added into the middle of the resistor string as shown in Figure 3. When Cnt0=L, Cnt1=L, Cnt2=L and Csw=H are provided to this circuit, the DAC will work in a normal mode that is the same as in Figure 1.

When the DAC is tested, test vectors are provided. The test vectors of the DAC shown in Figure 1 are shown in Table 1. It means that the number of test vectors of N-bits DACs is $2^{(N-1)}+1$.

Whenever each of the test vectors is provided, quiescent supply current is measured. If the measured current satisfies Eq.(3), the DAC is determined as faulty.

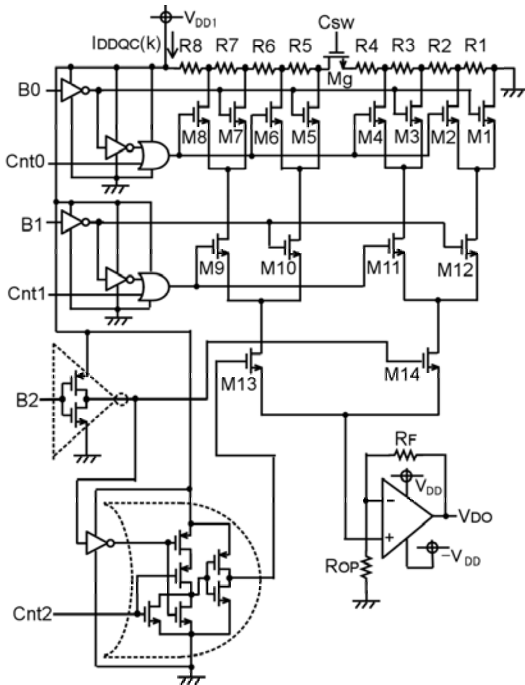

Figure 3. Current testable DAC

Table 1. Test vectors for DAC in Figure 3.

Test vector	B0	Cnt0	B1	Cnt1	B2	Cnt2	Csw
1	L	L	L	L	L	H	L
2	L	L	H	L	L	H	L
3	H	L	L	L	L	H	L
4	L	L	H	L	L	H	L
5	L	L	L	L	L	L	H

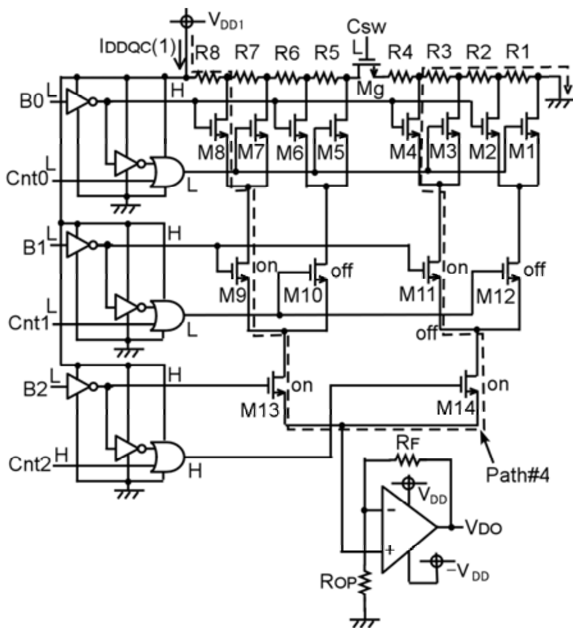

Figure 4. Supply current path for open detection.

When test vector #1 is provided to the DAC, if it is fault-free, supply current will flow through the current path, Path#4, in Figure 4. If an open occurs in the circuit elements on the path, the current will not flow and the circuit will be determined as faulty by means of Eq.(3).

Since application of our test vectors makes all of the current paths between V_{DD1} and GND flow once, all of the opens in the ADC will be detected.

Also, shorts may be detected by the test vectors. For example, if a short occurs at a resistor, some supply current change will appear, since resistance of the short is smaller than R_i. Thus the short will be detected by Eq.(3). Also, the short between the drain and the source of M10 will be detected as shown in Figure 5 owing to the elevated current along Path#5.

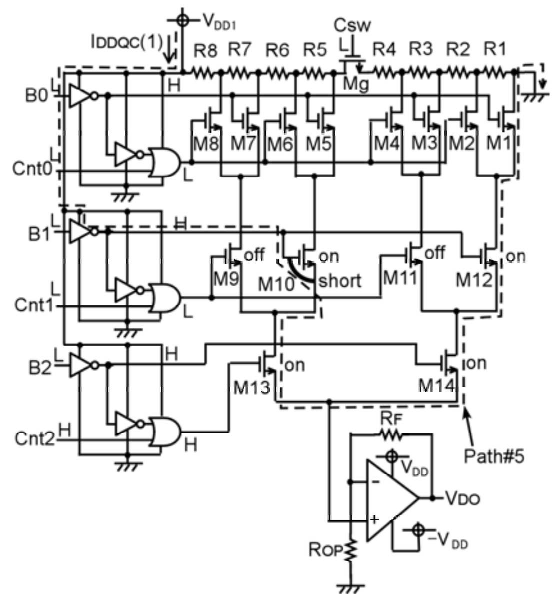

Figure 5. Supply current path of DAC having a short.

4. Evaluation of DFT

In order to evaluate testability of our testable DACs, we designed a 3 bits resistor string DAC and an 8 bits one with ES2 0.6μm CMOS process technology. The layouts are converted into Spice files and $I_{DDQC}(j)$ is derived for each test vector with PSpice. Opens and shorts are inserted in the same way as in the experiments for the circuit shown in Figure 1 that are denoted in section 2. $I_{th}(j)$ used in the experiments is 10% of $I_{DDQn}(j)$.

The obtained coverages are shown in Table 2. As shown in Table 2, all of the targeted opens are detected. All of the shorts in the resistor string of the 3 bits DAC are detected, while no shorts are detected in the string of the 8 bits DAC. That is the reason why the change of R_i caused by a short becomes small and the change in $I_{DDQc}(j)$ is smaller than $I_{th}(j)$ in the case of the 8 bits DAC. Also, for the same

reason as the tests of shorts in the resistor string, all of the shorts between drain and source terminals of MOSs are not detected in the 8 bits DAC. On the other hand, all of the opens in it are detected. Thus, it is expected that opens will be detected by introducing our DFT method.

Table 2. Defect coverage of DAC in Figure 3

		3bits DAC		8 bits DAC	
		open	short	open	short
resistor string		100%	100%	100%	0%
MOS	drain	100%	-	100%	-
	source	100%	-	100%	-
	drain-source	-	100%	-	24%
	drain-gate	-	100%	-	100%
	source-gate	-	100%	-	100%

5. Conclusion

In this paper, we have proposed a DFT method of resister string DACs so as for opens to be detected by supply current testing. It is shown experimentally that opens in resistor string DACs that are designed with the DFT method will be detected with a smaller number of test vectors than the exhausted ones.

Shorts in a resistor string DAC may not be detected even if our DFT method is introduced. We think that most of the shorts that are not detected by our current testing will be detected by measuring output voltage. It remains as a future works to evaluate coverage of a test method based on both supply current and output voltage.

Acknowledgment

This research is supported in part by Japan Society for the Promotion of Scientific under Grant in-Aid for Scientific Research(C)(No. 18500039).

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