A Design of High-Speed 1-Bit Full Adder Cell using 0.18 μm CMOS Process

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Abstract: With the recent development of portable system such as mobile communication and multimedia. Full adders are important components in applications of digital signal processors and microprocessors. We propose a new full adder with modified version of conventional ratioed logic and pass transistor logic. The proposed adder has the advantages over the conventional logic. The delay time is improved by 17% comparing to the average value and PDP(Power Delay Product) is improved by 19% comparing to the average value. The physical design has been evaluated using HSPICE.

1. Introduction

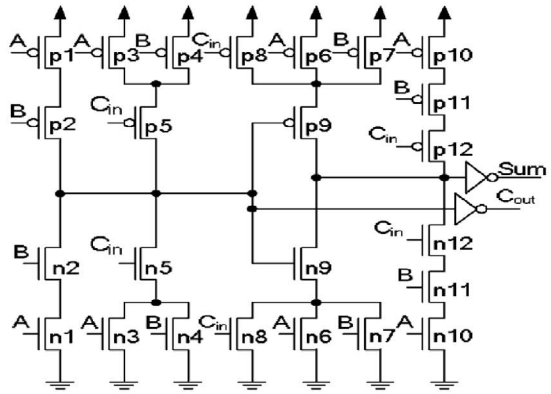
It is important to improve the power dissipation and operating speed for designing a full adder. The circuit delay is determined by the number of inversion levels, the number of transistors in series, and transistor sizes. Also the circuit size depends on the number of transistors and their sizes. Finally power dissipation is determined by the switching activity and the node capacitance. All these characteristics may vary considerably from one logic style to the other and is crucial for circuit designer to satisfy their needs.

In this paper, we categorize full adder designs in three categories based on their structures. And we present the design of a high speed 1-bit full adder based on a pass transistor logic and pseudo nMOS. The new adder is optimized for low PDP and is compared with the classical complementary CMOS[1], HPSC[2], TSAC[3].

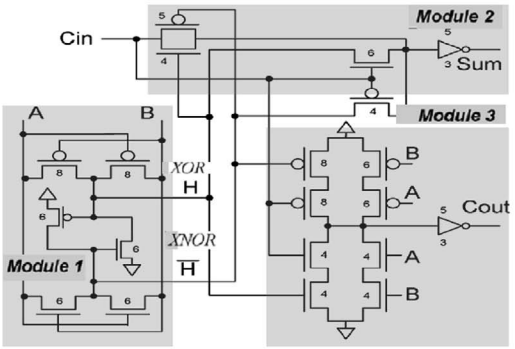
2. Standard Existing Full Adder Cells

The complementary CMOS full adder(C-CMOS) of Fig. 1(a) is based on the regular CMOS structure with pMOS pull-up and nMOS pull-down transistors. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of C-CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes. Moreover, the layout of C-CMOS circuit is straightforward and area-efficient due to the complementary transistor pairs and smaller number of interconnecting wires.

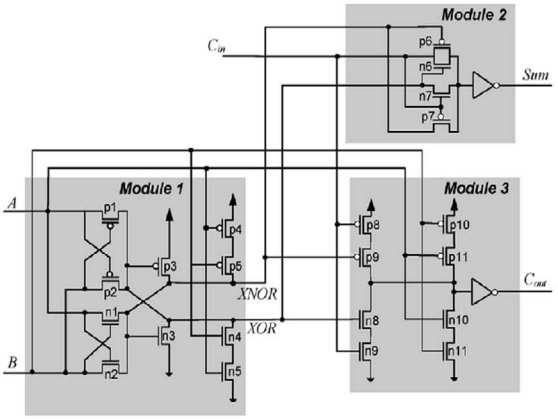
The HPSC is based on feedback logic, as shown in Fig. 1(b). HPSC has a feedback connection between XOR and XNOR function eliminating the non-full-swing operation.



(a) C-CMOS



(b) HPSC



(c) TSAC

Fig. 1 Standard existing full adder cells

The existence of Vdd and Gnd connections give good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component. However, when there is an input transition that leads to the input vector AB:00 or AB:11, there is a delay in switching the feedback transistors. This occurs because one of the feedback transistors is switched ON by a weak signal and the other signal is at high impedance state. This causes the increase in delay. As the supply voltage is scaled down, this delay tends to increase and eventually increase the PDP. To reduce this problem careful transistor sizing needs to be done to quickly switch the feedback transistors.

The TSAC full adder of Fig. 1(c) is based on the C-CMOS logic style. This circuit has inherited the advantages of C-CMOS logic style, which has been proven in to be superior in performance to all pass transistor logic styles for all logic gates except XOR at high supply voltage. Its robustness against voltage scaling and transistor sizing enables it to operate reliably at low voltage and arbitrary transistor size.

3. Full Adder Categorization

We categorize full adder cells in, broadly, three categories depending upon their structure and logical expression of the Sum output. The Sum and Carry outputs of a 1-bit full adder generated from the binary inputs A, B, and Cin can be generally expressed as

$$\begin{aligned} Sum &= A \oplus B \oplus Cin \\ Cout &= A \cdot B + Cin \cdot (A \oplus B) \end{aligned} \tag{1}$$

These outputs can be expressed in many different logic expressions and, thereby, determine the structure of the circuit. Based upon these different logic expressions, many full adder cells can be conceived. Moreover, the availability of different modules, as discussed earlier, provides the designer with more choices for a 1-bit adder implementation. We classify the different possible structures for full adder into three broad categories. These are as follows.

2. 1 XOR-XOR Base Full Adder

In this category, the Sum and Carry outputs are generated by the following expression, where H is A⊕B and H' is the complement of H. The general form of this category is shown in Fig. 2.

$$\begin{aligned} Sum &= A \oplus B \oplus Cin = H \oplus Cin \\ Cout &= A \cdot B + Cin \cdot H \end{aligned} \tag{2}$$

The Sum output is generated by two consecutive two-input XOR gates and the Cout output is the output of a 2-to-1 multiplexer with the select lines coming from the output of the first module. The first module can be either a XOR-XNOR circuit or just a XOR gate. In the first case, the H output of the XOR-XNOR circuit is XORed with the carry

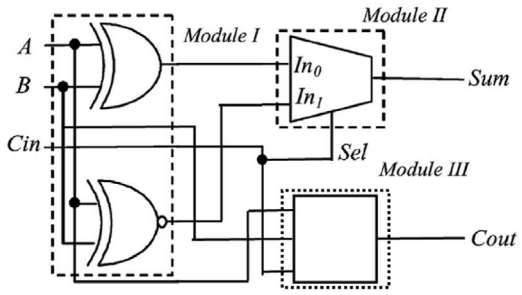


Fig. 2 General form of XOR-XOR based full adder

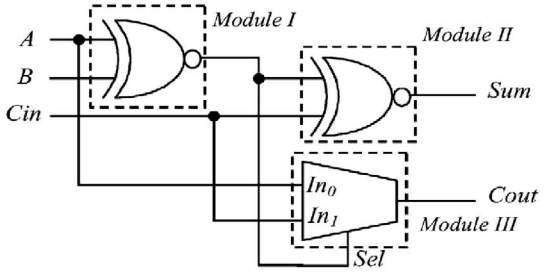


Fig. 3 General form of XNOR-XNOR based full adder

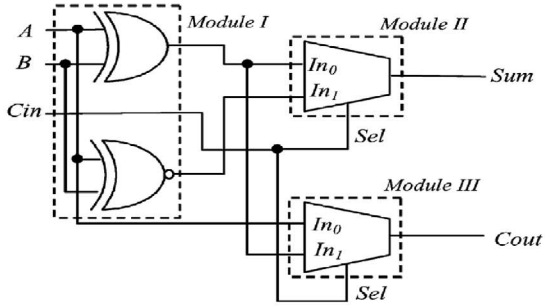


Fig. 4 General form of XOR-XNOR based full adder

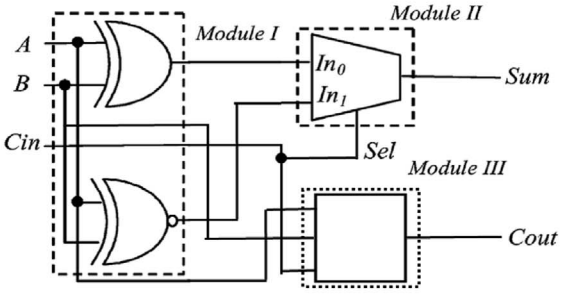


Fig. 5 Proposed full adder

from the previous stage(Cin) in module II. The H and H' ouputs are used as multiplexer select lines in module III. [4][5]

2. 2 XNOR-XNOR Based Full Adder

In this category, the Sum and Carry outputs are generated by the following expression. The general form of this category is shown in Fig. 3.

$$Sum = (H' \oplus Cin)'$$
$$Cout = A \cdot H' + Cin \cdot H \quad (3)$$

Module Ⅰ and module Ⅱ are XNOR gates and module Ⅲ is a 2-to-1 multiplexer. If the first module uses a XOR-XNOR circuit, then the H' output is XNORed with the Cin input to produce the Sum output. The static energy recovery full adder(SERF)[6] belongs to this category and uses a XNOR gate for module Ⅰ and Ⅱ and a pass transistor multiplexer for module Ⅲ.

2. 3 XOR-XNOR Based Full Adder

In this category, the Sum and Carry outputs are generated by the following expression. The general form of this category is shown in Fig. 4.

$$Sum = H \cdot Cin' + H' \cdot Cin$$
$$Cout = A \cdot H' + Cin \cdot H \quad (4)$$

Module Ⅰ is a XOR-XONR circuit producing H and H' signals and module Ⅱ and Ⅲ are 2-to-1 multiplexers with H and H' as select lines. The adder in [3] is an example.

2. 4 Proposed Full Adder

The proposed form of this category is shown in Fig. 5.

$$Sum = H \oplus Cin = H \cdot Cin' + H' \cdot Cin$$
$$Cout = A \cdot B + A \cdot Cin + B \cdot Cin \quad (5)$$

Module Ⅰ is an XOR-XNOR circuit producing H and H' signals and module Ⅱ is 2-to-1 multiplexers with H and H' as select lines. The output Cout of module Ⅲ is generated from A, B and Cin directly without passing through module Ⅰ as in conventional structure, Which results is high speed.

3. Proposed Circuits for Module Ⅲ

The proposed full adders can be divided into three modules. Module Ⅰ consists of either an XOR or XNOR circuit. Module Ⅱ and module Ⅲ generate Sum and Cout. The proposed circuit is shown in Fig. 6.

3. 1 Module Ⅰ

This circuit provides a full-swing operation and can operate at low voltages. The XOR-XNOR circuit is based on complementary pass-transistor logic using only one static inverter instead of two static inverters as in the regular CPL style XOR circuit. The first half of the circuit utilizes only nMOS pass transistors for the generation of the outputs. The cross-coupled pMOS transistors guarantee full-swing operation for all possible input combinations and reduce

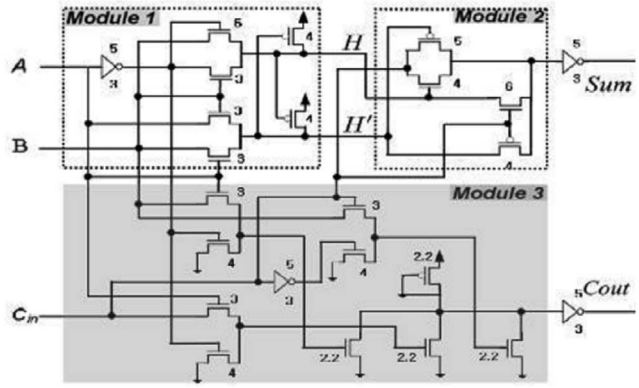


Fig. 6 Proposed full adder

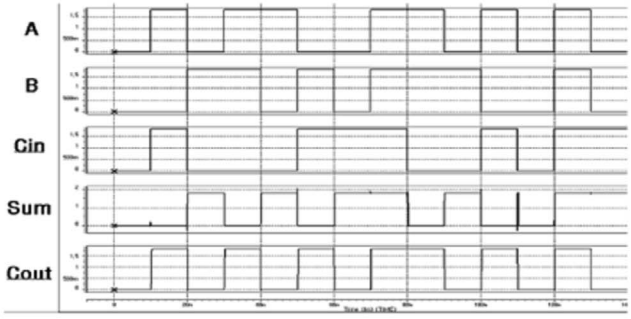


Fig. 7 Waveform simulation of proposed full adder

short-circuit power dissipation. The circuit is inherently fast due to the high mobility nMOS transistors and the fast differential stage of cross-coupled pMOS transistors.

3. 2 Module Ⅱ

These circuits are required to generate the Sum output given inputs H, H', and Cin. These circuits essentially perform the XOR or the XNOR function and can be used in the first module of the adder too.

Module Ⅱ is essentially the complement and has on inverter to produce Sum. This provides good driving capability due to the presence of the static inverter. This circuit is one of the best performers among all the circuits mentioned before in terms of signal integrity and average PDP. Both the circuits avoid the problem of threshold loss and have been widely used in adder implementation. We employ this for our full adder design.

3. 3 Module Ⅲ

We propose a circuit for module Ⅲ which uses the high speed pass transistor logic style and pseudo nMOS logic style. Pass transistor logic provides high speed, full-swing operation and good driving capability due to the output static inverters. Pseudo nMOS logic is referred to ratioed style. The advantage of pseudo nMOS is its high speed and low transistor count. On the negative side is the static power consumption of the pull-up transistor as well as the reduced output voltage swing, which makes this cell more susceptible to noise. To increase the output swing static an inverter is added to this circuit.

Table 1. Power, delay and PDP comparison of full adder

Adder	No. of Tr	Power (uW)	Delay (ns)	PDP (e-2)
CMOS	28	0.301	0.165	4.96
HPSC	22	0.250	0.141	3.52
TSAC	26	0.259	0.128	3.31
Proposed	28	0.261	0.119	3.10

4. Simulation Results

These circuits are design at the transistor-level in a standard 0.18 ㎛ CMOS process technology and comparison reported here uses HSPICE simulations to assess their performance. Some example waveforms for the inputs and outputs of the full adder are shown in Fig. 7. Simulation results for the examined full adder cells using the test circuit are shown in Table 1.

5. Conclusion

In this paper, a new high speed full adder circuit comprising general form of categorization is proposed. The proposed full adder has better performance than most of the standard full adder cells owing to the novels design modules proposed in this paper. The proposed 1-bit full adder has the advantages over the conventional complementary CMOS, HPSC, TSAC logic. The delay time is improved by 28% comparing to the complementary CMOS and improved by 16% to HPSC and improved by 8% to TSAC. PDP is improved by 38% comparing to the complementary CMOS and improved by 12% to HPSC and improved by 7% to TSAC.

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