PHY Adapter Layer Design for Low-power fast serial bus protocol

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Abstract: Interface used to connect chips is the main reason of EMI problem and requires excessive space of PCB to accomodate numerous parallel lines. UniPro uses a PHY layer for fast speed of transmission. PHY layer for UniPro generally uses a protocol with fast serial interface. Various approaches are being developed to implement the PHY layer. A PHY adapter can plug various PHY layers into UniPro protocol without modifications of data link layer of UniPro. In this paper, we design a PHY adapter that consists of power management unit and Rx/Tx buffers. The PHY adapter converts data from 2 pairs of data lane of PHY to 17-bit packet for upper layer. The PHY adapter is design in Verilog HDL and verified using ActiveHDL. The synthesis result shows that the gate count is 2,150 and the operation frequency is 199MHz.

1. Introduction

Recent improvements of multi-media IPs for mobile applications require an interface scheme to transmit large amount of data at fast rate with low power consumed. A multi-media device consists of CPU, graphic processor, memory, camera sensor and display module. Because each component has its own generic interface in parallel mode, PCB board is congested with a lot of interface lines and its physical area become large. The use of parallel lines for interface makes the EMI problem worse and consumes much power[1].

To overcome the disadvantage of parallel interface scheme, several fast serial schemes are tried. Mobile Digital Display Interface (MDDI) developed by Qualcomm is the one of such efforts. MDDI uses Low Voltage Differential Signaling (LVDS)[2] to achieve fast data transmission and low power consumption. However, the specifications of MDDI are limited to camera and display interfaces and cannot be generally applied to various system components.

UniPro protocol is a general protocol which can be applied to all the system components, i.e. camera, display, audio, and processor. UniPro is standardized by MIPI[3] and Figure 1 shows an example of MIPI interfaces. UniPro uses a PHY layer for fast speed of transmission. PHY layer for UniPro generally uses a protocol with fast serial interface. Various approaches are being developed to implement the PHY layer. Therefore, a layer between PHY layer and upper layer is needed. A PHY adapter can plug various PHY layers into UniPro protocol without modifications of data link layer of UniPro.

In this paper, we design the PHY adapter consists of power management unit and receiver buffer. The PHY adapter can support an effective power management method and manage 2 pairs of data lanes.

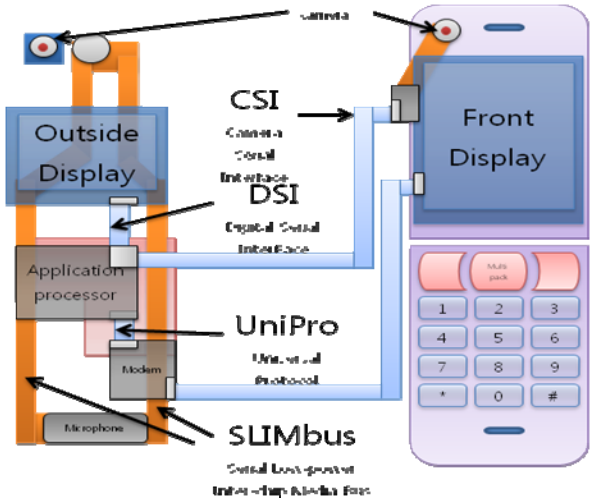

Figure . MIPI interfaces for mobile application

2. Layer Structure

PHY adapter layer functionally connects the physical layer and the data link layer as illustrated in Figure 2. PHY adapter consists of abstract physical protocol layer (APPI) and physical protocol layer (PPI). APPI supports 6 power modes by the power management unit and processes data stream from PPI by the receive unit. PPI can accommodate various PHY layers. In our design, the PPI can manage upto 2 data lanes and 1 clock lane.

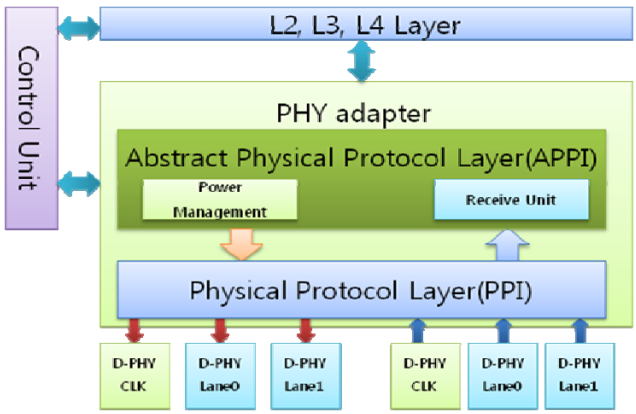

Figure . Block diagram of PHY adapter

The PHY adpater layer transmits and receives data in 17-bit symbols. The 17-bit symbols consist of one special ctrl bit and two bytes. This encoding scheme implies that the

number of encoded bytes transmitted by UniPro over the line will always be even because PHY adapter layer cannot send a partial 17-bit symbol. This is however, invisible at the application layer as UniPro groups bytes into packets which include a flag to invalidate the last byte in case the payload has an odd byte length. The D-PHY provides a 8 bits wide interface. The last remaining bit is transmitted in the next D-PHY symbol, together with the first seven bits of the next data link layer symbol, and so on. Figure 3 shows the mapping process.

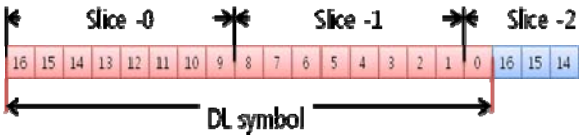

Figure . Symbol mapping process

In case of multiple lanes, the slices that are made through PHY symbol mapping are alternately assigned to one of the available lanes. The most significant bit (bit 16) of the first data link layer symbol is transmitted as first bit on lane 0. The end of an data link layer symbol stream can end in mid-byte. The associated bit-level time slots are filled with Ctrl_IDL symbols until real data becomes available or until the PHY is put into another power management state. Figure 4 shows the mapping process where the number of lane is 2.

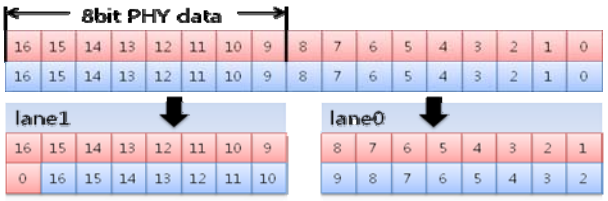

Figure . Transmission of 17-bit of symbols with two lanes

The frequency of clocks that are used to transmit data can be changed by the number of lanes that are supported[4]. Application clock is a normal clock that is used in each chip. Assume that the application clock is 200MHz, the DDR serial clock for D-PHY varies from 1.7G to 212.5MHz according to the number of lanes, as shown in Table 1. The byte clock is required to transmit one byte. The byte clock can be obtained by dividing the frequency of DDR Serial clock[5] by 4. Figure 5 shows clock relationships for 2 data lanes and 1 clock lane.

Table . Clocks used for PHY adapter

Clocks (MHz)	Number of lanes			
	8	4	2	1
Application clock	200	200	200	200
DDR Serial clock	212.5	425	850	1,700
Byte clock	52.9	106.3	212.5	425

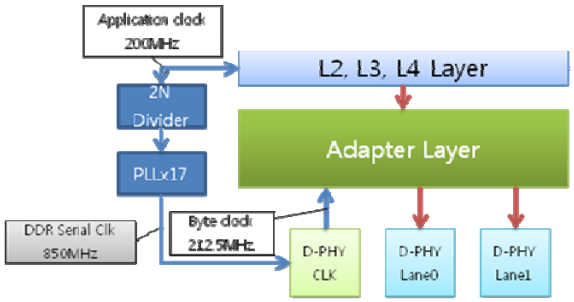

Figure . Clock relationships

There is a difference in data rate between the application clock used in upper layer and the byte clock used in the PHY layer. To transmit data safely, a buffer is used between the upper layer and the PHY adapter, as shown in Figure 6. The buffer accumulate symbol in sequence and shift unit selects symbol to be loaded to each lane.

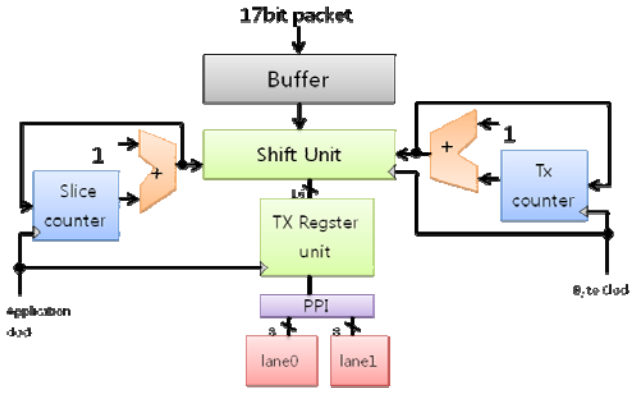

Figure . Schematic of Tx buffer

Figure . State transitions of power management state machine

States of the power management unit in PHY adapter are ON, SLOW, SLEEP, COMA, OFF, and COMA (ULP MODE) mode. Software sets power management[6] modes. The software power management modes drive the hardware to a specific state. Software cannot directly set a state. Each of these mode changes requires a hardware protocol to be executed in order to reach the desired state. Software can directly view the current state and, if desired, be interrupted when the state change actually occurs. When the link has reached the requested mode, the state in the status will be the same as the mode requested in the control register. Figure 7 shows the state transitions in the power management unit.

The ON mode is UniPro's highest performance and highest power mode. The link is always ready and provides the lowest latency of any UniPro mode. When data is not available idle symbols are transmitted. Figure 8 shows the waveform of packet transmission at ON mode

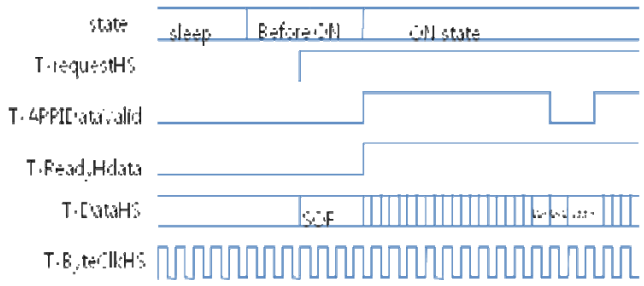

Figure . Transmisson of packets at ON mode

SLOW mode is a low power low performance mode. This mode can be used when the bandwidth requirements are very low. SLEEP mode is a low power mode that stops all activity on a link. A transmitter coming out of SLEEP mode can activate the corresponding receiver using a PHY-level protocol. The COMA modes lower power state when no communication is possible. It takes more time to exit from COMA than from SLEEP mode. A transmitter coming out of COMA mode can active the corresponding receiver using PHY-level protocols.

The AUTO modes provide autonomous power management. The link will transition from high power high performance mode to a lower power lower performance mode as required by the link usage. This mode allows the transmit side of the link to be in the high performance state, AUTO.HP, or in a lower power state depending upon bandwidth demands. The AUTO.HP state is used when the link has data to transfer. The AUTO.LP state is a lower power state that is used when the link does not have data to transfer. Figure 9 shows the block diagram related to AUTO mode.

Figure 10 shows a schematic block diagram of the receiver buffer. The RX_APPI_clk signal is generated from a frequency-divided RX_bitclk, which is turned on and off by the clock gate logic. In other words, the RX_APPI_clk is running at a slightly higher frequency than required, and paused once in a while, so that the averaged frequency matches exactly the incoming bitrate.

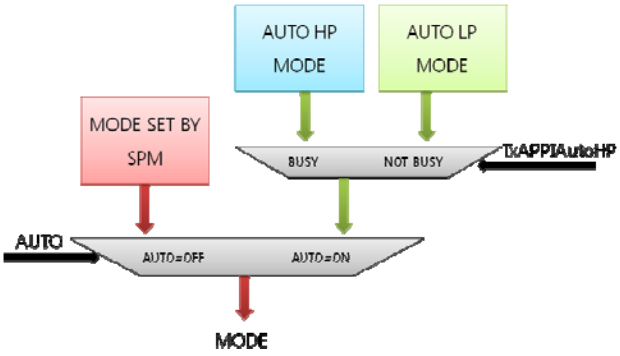

Figure . AUTO mode selection scheme

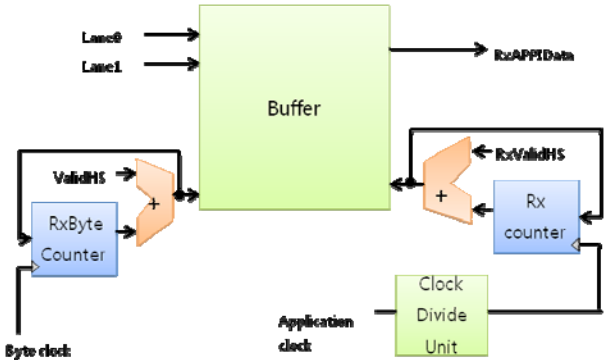

Figure . Receiver buffer block

3. Design and Simulation

Figure 11 shows the overall block diagram of the PHY adapter layer. Each power mode is controlled by the power management unit. Tx buffer and Rx buffer with line buffer[7] are employed for the synchronization of data from different clock. 16-byte register is used to provide the status and control the operation of the PHY adapter.

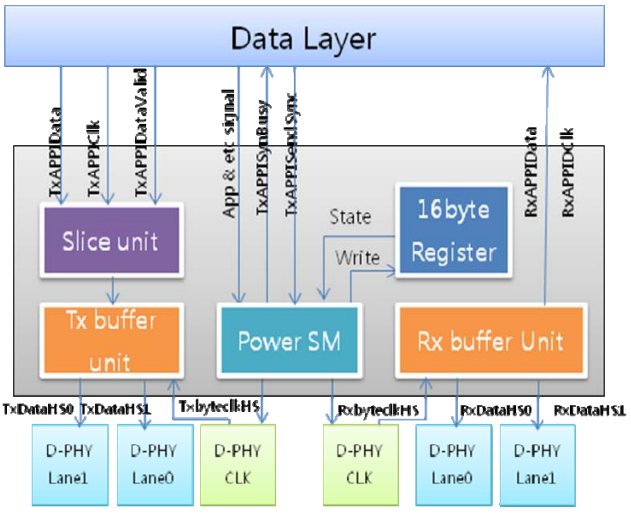

Figure . Overall block diagram of PHY adapter

The PHY adapter is design in Verilog HDL and verified using ActiveHDL. Figure 12 illustrates the waveform of data transmission. When TxRequestHS signal becomes high, the transmission of symbol starts. Data in lane 0 are transmitted through TxDataHS0, data in lane 1 through TxDataHS1.

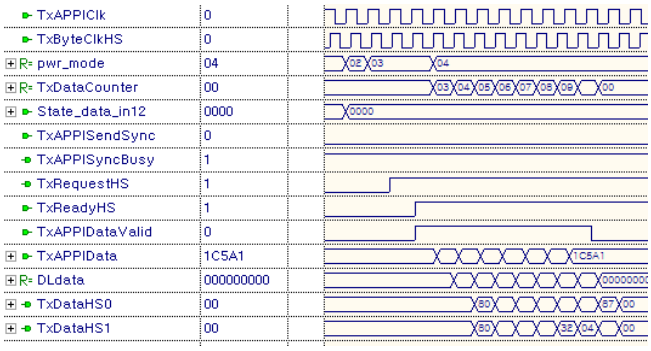

Figure . Transmission waveform

Figure 13 shows the waveform of data reception. Transmitted symbol is stored in line buffer (DLdata_RX) and then 17-bit packet is transmitted to upper layer.

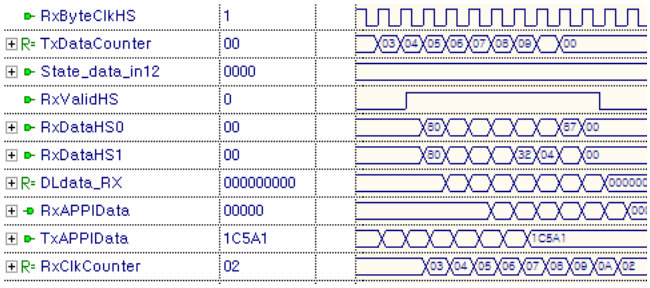

Figure . Data reception waveform

During the simulation the received data is stored in a result file to compare with original data. Then, pass or fail is automatically determined to validate the design. After the verification, the design was synthesized in 0.35 ㎛ CMOS standard-cell technology. Table 2 shows the result of synthesis. As results, the operating frequency is 199MHz and the gate count is about 2150.

Table . Synthesis result

Technology		0.35 ㎛ standard cell
Synthesis condition	Voltage	3.6 (typical : 3.3v)
	Process	0.7 (typical : 1)
	Temperature	-40 (typical:25)
Operating frequency		199 MHz
Gate count		2,150

4. Conclusion

In this paper, we designed the PHY adapter that can be used in UniPro. The power management unit in the PHY adapter provides 6 modes of power state for efficient power controls. Rx/Tx buffers are used to overcome the difference of clock frequencies. The PHY adapter can transmit and receive data by upto 2 lanes of data and the number of lane can change according to the amount of data. The PHY adapter was design to connect various PHY layers to the UniPro upper layers without modifications of the data link layer. The design is described by Verilog HDL and verified by ActiveHDL. After the verification, the synthesis result shows that the operating frequency is 199MHz and the gate count is about 2150.

Acknowledgments

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