A Design of 0.12ppm/Step Digitally Controlled Crystal Oscillator for PHS Application in 0.25μm CMOS Process

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Abstract: This paper presents a integrated Digitally Controlled Crystal Oscillator (DCXO) for PHS application. The frequency tuning is done by two-step MIM capacitor tuning scheme. The coarse tuning covers the frequency range of ±24ppm of the nominal frequency with the resolution of 0.75ppm. On the other hand, the fine tuning covers the frequency range of ±15ppm of the nominal frequency with the resolution of 0.12ppm. This chip is fabricated with 0.25μm CMOS technology, and the die area is 0.43mm x 0.55mm including PADs.

Keywords : DCXO, tuning range, fine, coarse, PHS

1. Introduction

PHS standards requires the mobile station (handset) to transmit signals with carrier frequency accuracy better than 0.5 ppm compared to the signals received from the base station. This accuracy is far beyond what even the best crystal oscillator can achieve without feedback correction.

PHS standards require 0.5 ppm frequency accuracy. This is achieved through the AFC loop in the digital baseband (DBB) that adjusts the frequency of the crystal oscillator based on the demodulated/decoded reference signals from the base station. The popular implementation, which uses an expensive external VCXO and provides the analog control voltage from the AFC DAC, is not cost and implementation effective [1].

A DCXO, therefore, provides an attractive alternative as it requires only an inexpensive external crystal and the controlled signal can be digitally derived from the DBB. The keys for a successful DCXO design are low phase noise, sub-1ppm of tuning step, and a wide monotonic tuning range to cover the crystal variations. Such a design is presented in this paper.

In an integrated VCXO, the frequency tuning is done by first converting the AFC digital signal to an analog signal, then driving an analog varactor. On the other hand, an integrated DCXO performs the frequency tuning by directly switching on/off the amount of capacitance required. The capacitance versus code transfer function is inherently linear. This linearity is only a weak function of PVT conditions.

In this work, a DCXO with a two-step MIM tuning capacitances is developed with a 0.25μm CMOS technology.

2. Architecture And Circuits

Figure 1 shows the block diagram of DCXO. It is composed of 19.2MHz Xtal, Negative-G_m circuit, coarse MIM tuning capacitance arrays that is controlled by 6 bits digital control signals (Coarse_Capsel<5:0>), fine MIM tuning capacitance arrays that is controlled by 256 bits digital control signals (Fine_CapSel<255:0>). The Negative-Gm can be controlled by the 2 bits control signals (Cur_Sel<1:0>).

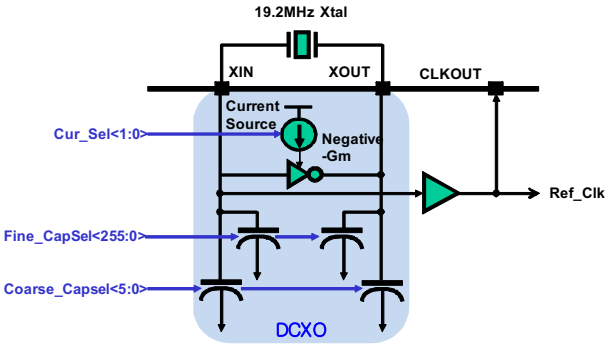

Figure 1. Block diagram of DCXO

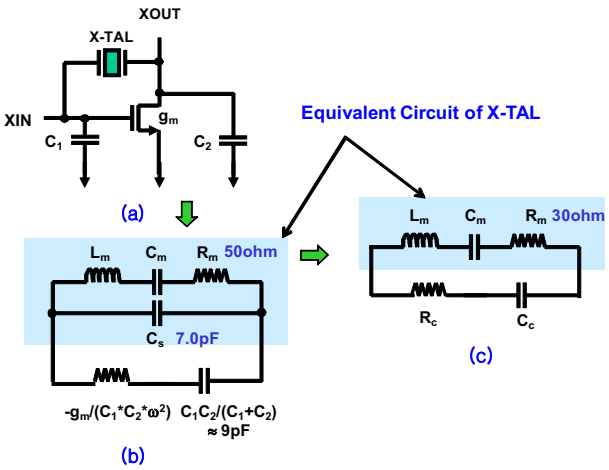

Figure 2. Equivalent circuit of DCXO.

Equivalent circuit of DCXO can be modeled as RLC networks shown in Figure 2. Equivalent resistance, R_c, and capacitance, C_c, can be represented as Eq. 1 and Eq. 2, respectively.

$$R_c = -\frac{g_m C_1 C_2}{g_m^2 C_s^2 + \omega^2((C_1+C_2)C_s + C_1C_2)^2} \quad (1)$$

$$C_c = \frac{g_m^2 C_s^2 + \omega^2((C_1+C_2)C_s + C_1C_2)^2}{g_m^2 C_s + \omega^2(C_1+C_2)((C_1+C_2)C_s + C_1C_2)} \quad (2)$$

We can get the range of g_m based on the equations, Eq. 3 - Eq. 8.

$$Z_c(g_m) = -\frac{g_m C_1 C_2}{(g_m C_s)^2 + \omega^2(C_1C_2 + C_2C_s + C_sC_1)^2} - j\frac{g_m^2 C_s + \omega^2(C_1+C_2)(C_1C_2 + C_2C_s + C_sC_1)}{\omega[(g_m C_s)^2 + \omega^2(C_1C_2 + C_2C_s + C_sC_1)^2]} \quad (3)$$

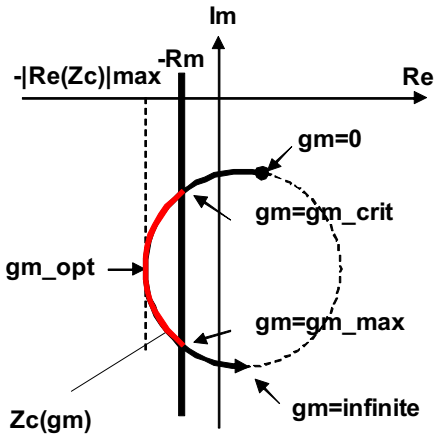

Figure 3. Plot of effective impedance as a function of g_m.

Figure 3 shows the plot of effective impedance as a function of g_m.

$$g_{m\_opt} = \omega\left(C_1 + C_2 + \frac{C_1C_2}{C_s}\right) \quad (4)$$

$$g_{m\_crit} = \frac{\omega C_m}{Q_p^2}\frac{(C_1+C_2)^2}{4C_1C_2} \quad (5)$$

$$Q = \frac{1}{\omega_m C_m R_m} \quad (6)$$

$$\omega_m = \frac{1}{\sqrt{L_m C_m}} \quad (7)$$

$$p = \frac{C_m}{2\left(C_s + \frac{C_1C_2}{C_1+C_2}\right)} \quad (8)$$

$$g_{m\_crit} \le g_m \le g_{m\_opt} \quad (9)$$

$$-R_c \ge R_m \quad (10)$$

The DCXO should meet the Eq. 9 and Eq. 10 for the stable oscillation.

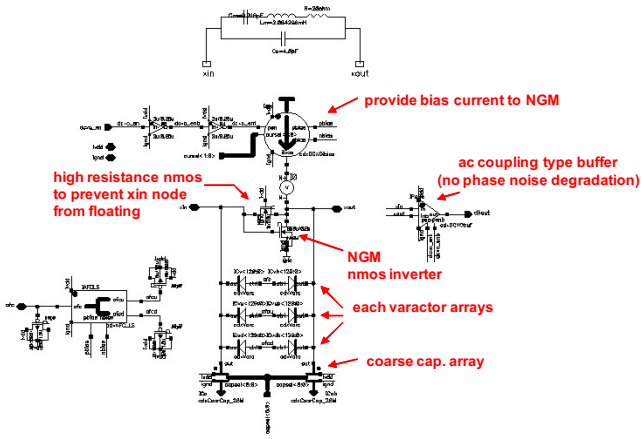

Figure 4. Schematic of DCXO.

Figure 4 shows the schematic of DCXO. It is composed of negative g_m, coarse cap array, and varactor arrays.

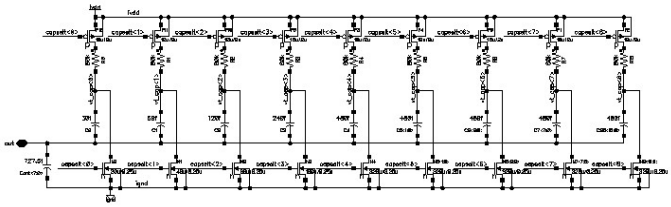

Figure 5. Schematic of coarse capacitor arrays.

Figure 5 shows the coarse capacitor arrays. It is composed of switches, capacitor, and resistors. The resistor is inserted to prevent the one of the capacitor nodes floating when they are not selected.

Table 1. Typical values of capacitor when Lm is 3.0mH

Freq.	Cap.	Cm	C1=C2
19.200307E+6	22.903542E-15	22.936375E-15	18.731687E-12
19.200288E+6	22.903588E-15	22.936421E-15	18.684977E-12
19.200269E+6	22.903634E-15	22.936467E-15	18.638401E-12
		Step:	46.576495E-15
Freq.	Cap.	Cm	C1=C2
19.200019E+6	22.904229E-15	22.937064E-15	18.044770E-12
19.200000E+6	22.904275E-15	22.937110E-15	18.000000E-12
19.199981E+6	22.904321E-15	22.937156E-15	17.955355E-12
		Step:	44.645414E-15
Freq.	Cap.	Cm	C1=C2
19.199731E+6	22.904916E-15	22.937753E-15	17.386103E-12
19.199712E+6	22.904962E-15	22.937799E-15	17.343153E-12
19.199693E+6	22.905008E-15	22.937845E-15	17.300321E-12
		Step:	42.831984E-15
		Minimun Step:	42.831984E-15

Table 1 shows the typical values of capacitor when L_m is 3.0mH.

3. Experimental Results

Figure 6 shows the chip microphotograph, and the die area is 0.43 x 0.55 mm^2 including PADs.

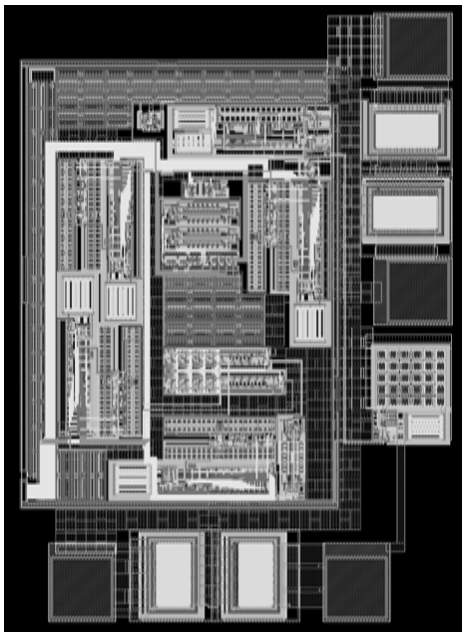

Figure 6. Chip microphotograph.

Figure 7 shows the transient simulation result of DCXO. The oscillator output is stable after about 100μs.

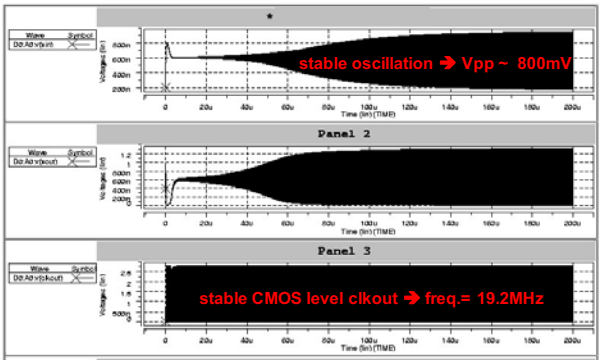

Figure 7. Transient simulation result of DCXO.

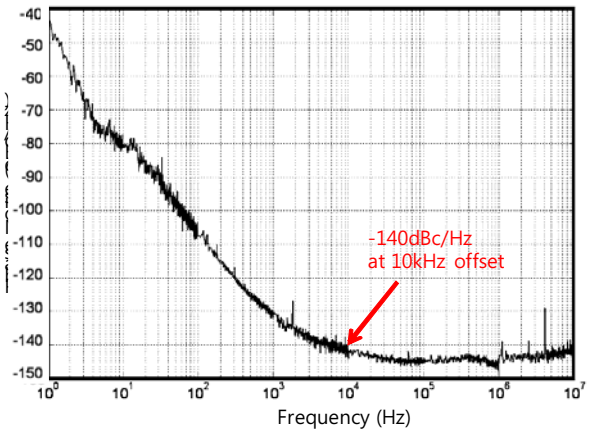

Figure 8. Measured phase noise of DCXO.

Figure 8 shows the measured phase noise of DCXO. It is about -140dBc/Hz at 1kHz offset.

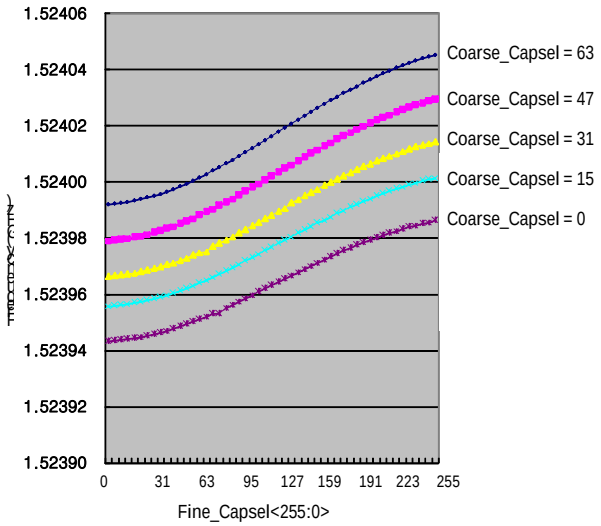

Figure 9. Measured DCXO frequency versus AFC code transfer function.

Figure 9 shows the measured DCXO frequency versus AFC code transfer function. The frequency is measured at the output of VCO to increase the measurement accuracy. The frequency tuning range that can be covered with Fine_Capsel<255:0> is 30ppm with the resolution of 0.12ppm. The frequency tuning range that can be covered with Coarse_Capsel<5:0> is 48ppm with a resolution of 0.75ppm.

Table 2 summarizes the tuning range specification of DCXO for PHS applications, and the designed DCXO can meet the specification.

Table 2. Tuning Range Specification of DCXO for PHS application

Frequency tolerance caused by	Range
Unit variation (at room temperature)	+/- 22ppm
Temperature variation (-30~80 °C)	+/- 15ppm
Aging (2ppm/year)	+/- 9ppm
Total	+/- 46ppm

Acknowledgement

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References

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