

Design of Low Noise Dualband CMOS RF Front-end for IEEE 802.11n

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Abstract: A dualband low noise RF front-end is designed in 0.18 μ m CMOS technology. The operation frequency is selected by turning on and off the switched inductor and capacitor. By using the self-matched capacitor, simultaneous input and noise matching can be easily achieved in 2 GHz and 5 GHz band. Proposed RF front-end has the good performances because self-matched capacitor helps reducing the number of switchable components which can cause the noise and loss in circuit.

1. Introduction

802.11n standard builds upon 802.11a/b by adding MIMO operation for high data rate. 802.11n receiver should satisfy the wide range of requirements such as frequency band, dynamic range and bandwidth etc, because it can support previous 802.11 standards series. This receiver should selectively support 2.4 GHz and 5 GHz bands; 20 MHz and 40 MHz channel bandwidth. Also, the receiver should be comparable with a single standard receiver in size, cost, and numbers of RF components.

Most previous multi-standard wireless receivers used independent RF front-end for each standard. It increases cost, size and weight of system as the number of target standards increases. Therefore, the research trend is changed from multi-path transceiver to multi-standard transceiver closer to SDR for reusing of components. Previous multi-standard receiver is categorized as concurrent, wideband and tunable matching design technique. Wide-band matching design technique [1] is similar to wide-band filter design method. By controlling pole and zero of the network's transfer function, it supports simultaneously all desired frequency band. The concurrent matching design technique [2] can be operated in two or three mode simultaneously by adding LC resonant circuit. However, these two methods are not reconfigurable and suffer from spurious responses, because of non-exclusive acceptance within its operation range. In tunable matching receiver, operation frequency is selected by active inductor and capacitor. They are the most flexible components. Since active capacitor has the small tuning range, it is not sufficient to support wide range of frequency by only using active capacitor. Variable active inductor provides wide tuning range and it has advantage over spiral inductor in terms of Q factor and area, but it increases power consumption [3]. Moreover, by using the active components, it can degrade the linearity and noise characteristics of circuits.

In this paper, a dualband CMOS RF front-end is presented. The self-matched capacitor and switched inductor can provide simultaneous input and noise matching in 2 GHz and 5 GHz band. The performance of

dualband RF front-end is within the specification of target standard.

2. Front-end design and operation principle

To select operation frequency, switched inductor is adopted in input matching network. This matching network is completed by adding an inductor with a switch in front of the existing matching network for high frequency. Figure 1 shows switched inductor input matching network and its equivalent circuit. The selection of frequency can be achieved by turning on or off the switch transistor (M_S). When the switch is turned off, matching network operates in low frequency mode. Then, the matching network acts like a series connection of L_1 , C and L_2 . On the other hand, high frequency mode is realized by turning on the switch transistor. In this case, matching network acts like a series circuit of L_2 and C.

The switch transistor can be modeled simply by a channel resistance (R_{sw}) and two parasitic capacitances (C_p). It is assumed for convenience that C_{gs} and C_{gd} of M_S are the same although they are not exactly same with each other. When M_S is turned off, R_{sw} is very large. Otherwise, when M_S is turned on, R_{sw} becomes very small and follows Eq. (1).

$$R_{sw} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{th})} \quad (1)$$

As the V_{GS} and size of M_S become larger, R_{sw} becomes smaller when other conditions are the same. Also, NMOS is more useful to reduce the value of R_{sw} than PMOS because of high mobility. Large transistor results in large C_p and small R_{sw} ; the small transistor results in small C_p and large R_{sw} . When M_S is turned off, R_{sw} is larger than 10 M Ω . The value of $C_{p,on}$ when SW is turned on is larger than the value of $C_{p,off}$ when SW is turned off.

The insertion loss is related to R_{sw} and C_p . When both R_{sw} and C_p become small, the insertion loss becomes small. However, it is impossible to be small both R_{sw} and C_p at the same time. The insertion loss in low frequency mode (SW off) is determined by value of $C_{p,off}$. The insertion loss by $R_{sw,off}$ is negligible, because its value is very large and it is connected parallel to signal path. Therefore small size of C_p is more desirable. Otherwise, the insertion loss in high frequency (SW on) is affected by not only value of $C_{p,on}$, but also the value of $R_{sw,on}$ because RF signal passes through the channel resistance ($R_{sw,on}$) of M_S . To reduce the signal loss, both $C_{p,on}$ and $R_{sw,on}$ should be as smaller as possible. If large size of switch is chosen to reduce the value of $R_{sw,on}$, $C_{p,on}$ becomes larger. There is trade-off

between value of R_{sw} and C_p with respect to transistor size. Therefore, the size of switch transistor has to be chosen carefully.

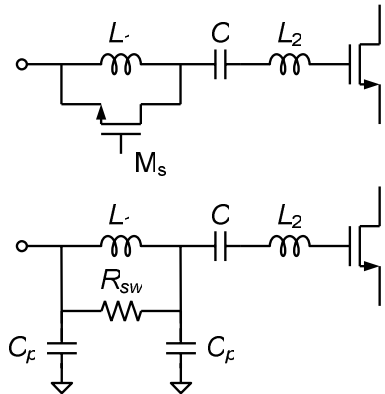


Figure 1. Switched inductor input matching network and its equivalent circuit

Figure 2 shows the schematic of the proposed dualband RF front-end. To select the frequency, a switched inductors and switched capacitor are used in input stages and interstage, respectively. When M_s in input stage is turned off and M_F in interstage is turned on, the front-end is operated in 2.4 GHz and has lower noise characteristics. When M_s is turned on and M_F is turned off, the front-end is operated in 5 GHz bands. In interstage matching network, larger capacitance is advantage to match in lower frequency band with the same inductor. Therefore, when it support in 5 GHz band, M_F should be turned off for small capacitance. Contrary to input matching network, an inductor and switched capacitor can be used in interstage for small chip size [4]. It can be possible because output stage is related to only power gain, and sufficient power gain can be obtained by switched capacitor in low and high frequency mode. As reducing the number of inductor in output stage, the size of designed LNA can be small to comparable with single standard LNA. The LNA is designed with the conventional cascode topology for high port isolation. The size of M_s and M_F should be chosen carefully because the size of switch determines the insertion loss by channel resistance and parasitic capacitance of M_s . The double-balanced Gilbert cell architecture is used for port isolation and high linearity. In direct conversion receiver, flicker noise and even order linearity are the most important factors. Fully differential architecture is helpful to eliminate even order nonlinearity. Since flicker noise is directly proportional to amount of current in the differential switching quads, it is minimized in there as well as the swiching quads are designed with large size. Since 802.11 series which use OFMD modulation do not use the subcarrier near the DC, DC offset is not considered.

Input impedance Z_i is expressed as

$$Z_i = \frac{1}{j\omega(C_{self} + C_{gs})} + j\omega L_s + j\omega \frac{C_{gs}^2 L_g}{(C_{self} + C_{gs})(C_{self} + C_{gs} - C_{self} C_{gs} L_g \omega^2)} + \frac{\frac{\omega_c g_{m0}}{\omega_c + \omega} \cdot L_s}{(C_{self} + C_{gs} - C_{self} C_{gs} L_g \omega^2)} \quad (\because g_m = \frac{g_{m0}}{1 + \frac{\omega}{\omega_c}}) \quad (1)$$

Imaginary part of Z_i is canceled by conjugate matching according to the operation frequency. Real part of Z_i should be matched to 50Ω to reduce the signal loss. The numerator of $\text{Re}[Z_i]$ in Eq. (1) may be decreased as the frequency increased because of g_m [5], and denominator of $\text{Re}[Z_i]$ is decreased as the frequency increases because there is ω^2 term. Finally, real part of Z_i can be maintained to 50Ω in all target frequency bands by determining suitable value of components.

Figure 3 shows the variation of real part of Z_i with and without C_{self} . Real part of Z_i with C_{self} has the smaller variation according to the frequency than real part of Z_i without C_{self} .

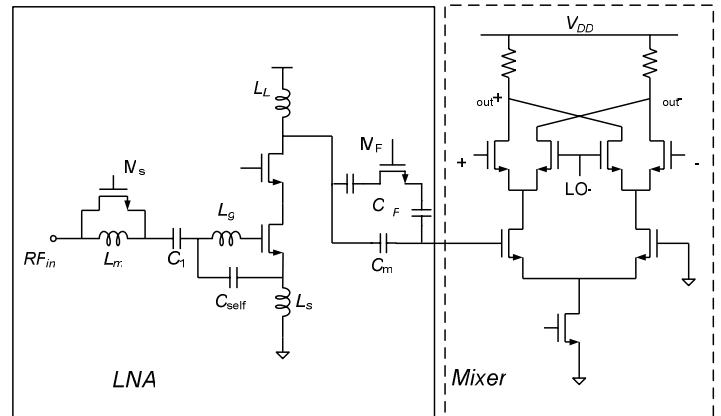


Figure 2. The schematic of designed dualband RF front-end

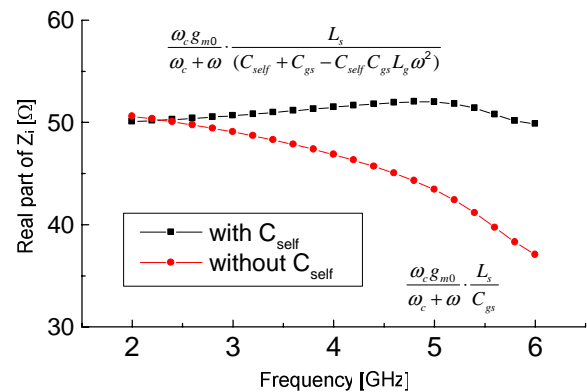


Figure 3. The variation of $\text{Re}[Z_i]$ according to the frequency

3. Simulation result

Proposed RF front-end is designed in 0.18 um CMOS process. Figure 4 shows the input return loss of proposed RF front-end in low and high frequency modes. The input return losses are less than -15 dB, and the gain of front-end is higher than 30 dB in 2.4 and 5.8 GHz. By turning on and off the switch, reflection coefficient and return loss is changed. C_{self} is useful for obtaining high gain as well as it helps the impedance and noise matching. Designed LNA can have high gain because the small numerator of real part of Z_i in Eq. (1) can make it possible to design with small L_s . As shown in Figure 5, NF of RF front-end is less than 2.6 dB in both band. Proposed RF front-end has the good noise characteristic in 5 GHz band because C_{self} make it easy to noise matching in dualband, and considering the performance degradation, characteristics of noise is focused on 5 GHz. In direct conversion receiver, filcker noise is one of the important performance. However, it is not a serious problem in 802.11n system because OFDM does not use of subcarrier near the 0 Hz. In this system, significant frequency is larger than 100 kHz. Power consumption of designed front-end is 10.2 mW with the 1.8 V supply voltage. Figure 6 shows the die-photo. Chip size is 0.7×1.1 mm². -11 and -17 dBm of IIP3 is obtained in 2.4 and 5.8 GHz, respectively. Other performances are summarized in Table 1.

Table 1. Performance summary

Frequency [GHz]	2.4	5.1~5.9
Current [mA]	5.7	
Supply Voltage[V]	1.8	
Gain [dB]	32	31
Noise Figure [dB]	2.6	2.5
IIP3[dBm]	-11	-17
Technology	0.18 um CMOS	

4. Conclusion

A dualband RF front-end is designed in 0.18 um CMOS technology. The band selection is achieved by turning on or off switch transistor. Self-matched capacitor helps simultaneous impedance and noise matching in 2 GHz and 5 GHz. If their real values of input impedance are different, they need different extra capacitors and switches. C_{self} is useful for getting the high gain and good performance because it solved above problem. The performance of proposed dualband front-end is suitable for supporting 802.11n standard. I measured the performance in 2.4 GHz and I did not measure yet in 5 GHz.

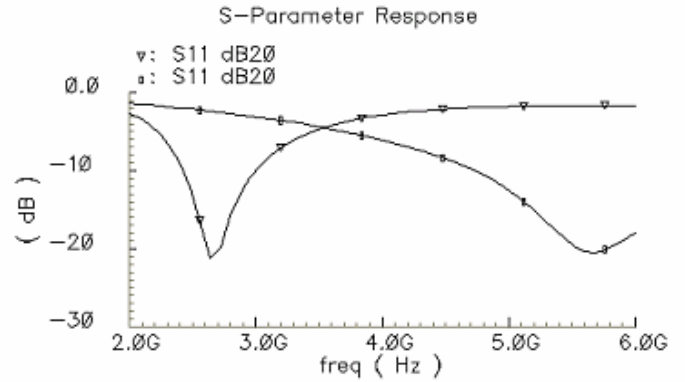
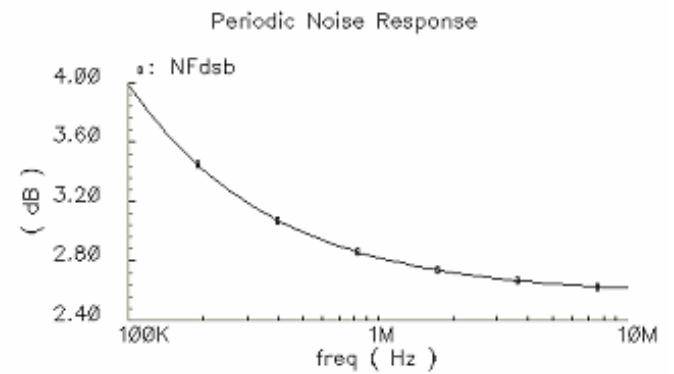
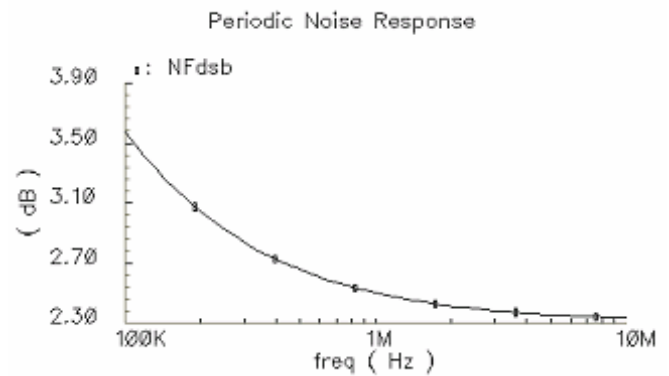


Figure 4. Input return loss of RF front-end



(a) Noise figure in 2.4 GHz band



(b) Noise figure in 5.2 GHz band

Figure 5. Noise figure in 2 and 5 GHz band

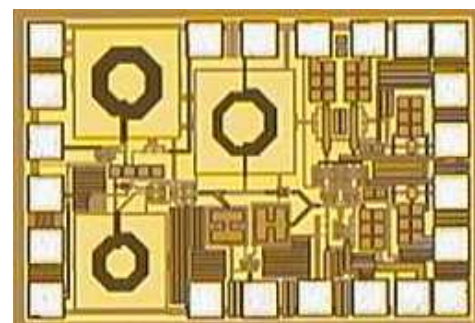


Figure 6. The die-photo of dualband RF front-end

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