

## A Study on the Design of the On-Chip 2.5V-to-1.0V VDC for Semiconductor Devices

Hae-Jun Seo<sup>1</sup>, Young-Woon Kim<sup>2</sup>, and Tae-Won Cho<sup>3</sup>

School of Electrical and Computer Engineering, Chungbuk University, Korea

Gaeshin 12, Heungduk, Cheongju, Chungbuk, Korea

Tel: +82-43-261-2479, Fax: +82-43-266-2479

E-mail: <sup>1</sup>hjseo@dsc.cbnu.ac.kr, <sup>2</sup>ywkim@dsc.cbnu.ac.kr, <sup>3</sup>twcho@cbnu.ac.kr

**Abstract:** This paper proposes a new on-chip voltage down converter(VDC), which employs a new reference voltage generator(RVG). The converter adopts a temperature-independence reference voltage generator, and a voltage-up converter. The architecture of the proposed VDC has a high-precision, and it was verified based on a 0.25  $\mu\text{m}$  1P5M standard CMOS technology. For 2.5V to 1.0V conversion, the RVG circuit has a good characteristic such as temperature dependency of only 0.2mV/ $^{\circ}\text{C}$ , and the voltage-up circuit has a good voltage deviation within 0.12% for 5% variation of supply voltage VDD. The output voltage is stabilized with 1mV for load current varying from 0 to 100mA.

### 1. Introduction

Recently, supply voltage is scaling down because of reducing oxide thickness and increasing demand for low-power portable equipment. Currently, 3.3V power supplies are commonly used; soon, circuits operating with 1.2V or less will be introduced. Voltage down conversion eliminates multiple supply voltage pins from memory device packages and extra power supply circuits. Low internal voltage makes it possible to lower internal signal levels enhancing device reliability and provides with more stable characteristics for temperature changes and process variations.

The designs of voltage down converters are to meet the differences in current profiles of storage arrays and peripheral circuitry. The voltage down converter for storage arrays aims at stability with high but isolated change in driving current bursts. The one for peripheral circuitry handles lower and more frequent current bursts. It would be more convenient to design voltage down converters separately for storage arrays and peripheral circuitry.

Two design concerns are reported in voltage down converter circuits: low power consumption and stability in operation. A lower voltage operation brings substantially lower power consumption since the power consumption is proportional to the square of the operating voltage. Then, the stability issue of a voltage down converter reports the minimal voltage changes due to some operational disturbances such as external supply voltage fluctuations, abrupt internal current surge and temperature changes. It helps to get normal operations under some external power supply voltage fluctuations, say 10%, without excessive additional circuitry. Without circuitry having some slight voltage increase along the ambient temperature, memories typically experience slower access. It is also to allow some tolerance on internal voltage affected by

parameter variations during a silicon fabrication process [1]. These are the reasons, in semiconductor memory devices, to achieve both low power operation and stability in operation, of which an on-chip DC-to-DC voltage down converter(VDC) is strongly desired.

In this paper, we propose a voltage-up circuit based VDC. Employing a bandgap reference(BGR) based on vertical parasitic bipolar in n-well, the circuit achieves good insensitivity characteristics of temperature and external supply voltage. Therefore, it is suitable for the low-power memory chips.

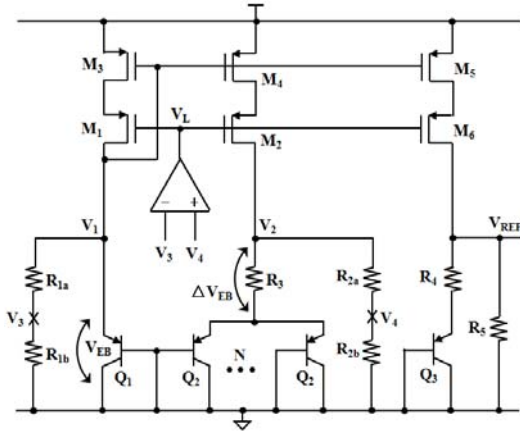
### 2. Design and Analysis of VDC

A voltage down converter for converting an external power voltage into an internal power voltage and providing the internal power voltage to an internal circuitry comprising is defined by: a reference voltage generation means for receiving the external power voltage and generating a constant reference voltage where variation of the external power voltage and change of circumstance temperature are compensated; a reference voltage converting means for converting the reference voltage from the reference voltage generation means into a reference voltage for stress mode or a reference voltage for normal mode; and a driving means for receiving the references to generate the internal power voltage required to operation of the internal circuitry. The basic blocks of the conventional VDC include a start-up, a reference voltage generator, a voltage-up converter, and a pass device circuit with low output impedance and large driving capability [2][3].

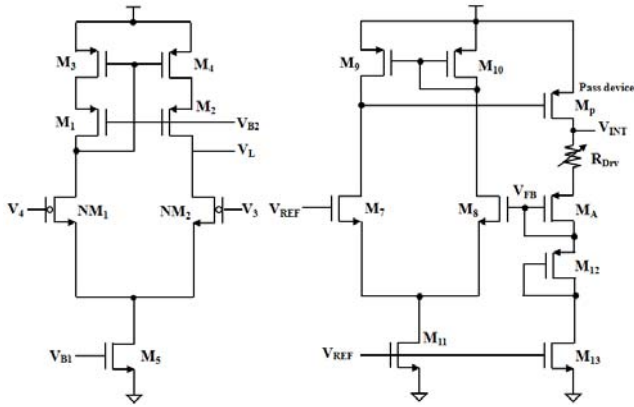
This paper relates to a circuit for generating a reference voltage in a semiconductor device and particularly to an internal voltage down converter which produces an internal supply voltage by down-converting an external supply voltage.

#### 2.1 Design of proposed VDC

Two aspects are important in voltage down converter design: lower impedance of power supply node and stabilization of the DC output level. It is difficult to an optimized design for both design concerns at the same time. Two different approaches are employed to meet these design variables: internal voltage source and reference voltage source. An internal voltage source is designed primarily aiming at lower output impedance so that it can supply constant current on loads with varying impedance. A design of a voltage reference source, on the other hand, concentrates to overcome variations in external operational conditions such as external supply voltage fluctuations and



(a) Proposed RVG circuit



(b) Wide-swing differential amplifier (c) Voltage-up circuit

Fig. 1 Proposed VDC circuit

temperature changes. A successful voltage down converter is to take advantages of these two different design approaches.

## 2.2 Analog of proposed VDC

Fig. 1 is the circuit of proposed VDC, which is composed of a reference voltage generator based on bandgap reference, and a voltage-up circuit with low output impedance and high-driving capability. The function of the RVG is to produce a stable reference voltage  $V_{ref}$  that is free from fluctuations of external supply voltage  $V_{DD}$  and temperature. The proposed bandgap RVG circuit consists of a CMOS wide-swing differential-amplifier, parasitic BJTs, and resistors. The voltage-up circuit consists of a differential amplifier, a  $M_p$  pass device and a level-shifter consists of a  $M_A$  pMOS device, a  $R_{Drv}$  driving resistor and two MOSFETs  $M_{11}$  and  $M_{12}$  for voltage feedback. The wide-swing differential amplifier adjusts the internal supply voltage  $V_{int}$  level to match the  $V_{int}$  shift level with the  $V_{ref}$  level. Because of the high drivability requirement of VDC, the pass device size of  $M_p$  is relatively large.

Major concerns of bandgap reference circuit designs are to obtain a stable voltage level even with power supply fluctuation, process parameter scattering and ambient temperature variation. Various circuit innovations are applied to keep an accurate and precise voltage level at the

output of a reference voltage generator. We now review some of representative designs in terms of stability and immunity against power and junction temperature changes.

In this design some modifications are made to the circuit of conventional RVGs[2]. The main differences are that an amplifier with a nMOS input stage is used and the inputs of the amplifier are connected to native nMOS stage instead of pMOS input stage. The resulted circuit is shown in Fig. 1(b). In addition, the output impedance of the current sources is improved by adding cascode devices. This is important in order to reduce the supply voltage sensitivity of the voltage  $V_{ref}$ . When the sum of the voltages across  $R_{1a}$  and  $R_{1b}$  is equal to  $V_{EB1}$ , the voltage with respect to ground at  $V_3$  and  $V_4$  is  $(R_{1b}/(R_{1a}+R_{1b})) \cdot V_{EB1}$ .

$$VDD_{min} = \max(V_{EB1} \times \left( \frac{R_{1b}}{R_{1a} + R_{1b}} \right) - |V_{TNM, NM1}| + |V_{DSAT, MP3}|, V_{ref} + |V_{TP, MP5}|) \quad (1)$$

In the original design the operational-amplifier(op-amp) inputs are connected to the voltages  $V_1$  and  $V_2$  that are roughly in 0.4V-to-0.6V level, which is not a suitable input for an op-amp in a 1V-to-2.5V design. To overcome that the resistors  $R_1$  and  $R_2$  are divided into two series connected parts. Now the voltages  $V_3$  and  $V_4$ , which are nominally set between 150 and 200mV, are in proper range for an op-amp with pMOS input transistors.

Fig. 1 (b) illustrates the structure of the native nMOS, which is easily fabricated by CMOS option process. The transistors, with  $V_3$  and  $V_4$  applied to the gates, are native nMOS transistors ( $V_{TH} = -0.15V$ ) because the threshold voltages of the enhancement-mode nMOS transistors exceed  $V_{-feedback}$  in the standard 0.25  $\mu m$  CMOS process.

A current which is proportional to the absolute temperature(PTAT) is generated and added into a base-emitter voltage of  $Q_3$ . From Fig. 1(a),  $M_1 \sim M_6$  form cascode current mirrors which can operate for lower supply voltage. The amplifier enforces  $V_3$  and  $V_4$  to have equal potential. As a result,  $V_1$  and  $V_2$  also have the same potential when  $R_{1a} = R_{2a}$  and  $R_{1b} = R_{2b}$ . Therefore, generated current is given by

$$I_{current} = \frac{V_T \cdot \ln N}{R_3} + \frac{V_{EB1}}{R_1} \quad (2)$$

where  $N$  is the emitter area ratio,  $V_T$  is the thermal voltage, and  $R_1 = R_{1a} + R_{1b} = R_2 = R_{2a} + R_{2b}$ . The current  $I$  is injected to  $R_4$  by the current mirror formed by  $M_3$ ,  $M_4$ , and  $M_5$ , and this gives the reference voltage as follows:

$$V_{ref} = V_{BE3} + \frac{R_4}{R_2} \cdot \left\{ V_{EB1} + V_T \cdot \left( \frac{R_2}{R_3} \ln N \right) \right\} \quad (3)$$

A scaled-down bandgap reference voltage can be obtained by an appropriate resistor ratio of  $R_4$  to  $R_2$ . Moreover, trimming on the resistor ratio (ratio of  $R_2$  to  $R_3$ ) to achieve a good TC can be done on  $R_{1a}$  and  $R_{2a}$  simultaneously. This structure is suitable for any CMOS technology to implement low-voltage bandgap reference.

The proposed voltage-up circuit is shown in Fig.1 (c). The voltage-up circuit can be converted the output voltage of bandgap reference  $V_{ref}$  into a higher internal supply voltage  $V_{INT}$ . And it should have enough current supply capability and low output impedance so that the  $V_{INT}$  is not very much affected by the large loading current fluctuation. So the size of pass device  $M_P$  is relatively large.

The circuit is composed of a feedback amplifier and a  $M_P$ ,  $R_{DRV}$ ,  $M_A$ ,  $M_{12}$ , and  $M_{13}$ , which plays an important role in obtaining further accuracy in the output voltage of the voltage-up circuit. The output voltage  $V_{INT}$  is  $I_{PTAT} \cdot R_{DRV} \cdot V_{TPA} + V_{TP12} + V_{SAT13}$  where  $V_{TPA}$  is the built-in voltage of the threshold voltage of pMOS device. To minimize the voltage error of  $V_{INT}$  from the nominal value  $V_{DD}$  for a maximum  $V_{ref}$ -range, the trimming characteristics should be designed such that any two adjacent lines pass through points  $(V_{ref}, V_{DD} - \Delta V_{INT})$  and  $(V_{ref}, V_{DD} + \Delta V_{INT})$ , as suggested by the vertical broken lines in Fig.1(c).

$$V_{INT} - | (I_{PTAT} \cdot R_{DRV}) + V_{TPA} + V_{TP12} + V_{TP13} | \quad (4)$$

$$= \left[ 2 \sqrt{\frac{\beta_2}{\beta_1} + 1} \right] \cdot [V_{ref} - |V_{TPA}|]$$

### 3. Simulation Results

The proposed on-chip VDC is designed to provide a constant DC voltage around 1.0V with external supply voltage of 2.5V. Also, the proposed RVG can be successfully lowered in the HSPICE simulation when the threshold voltages are optimized for a low-voltage and a wide-range voltage operation. The proposed VDC is designed with a 0.25  $\mu\text{m}$  CMOS technology.

#### 3.1 Simulation results of VREF

For the temperature effects, the simulation results are shown in Fig.2. Here, in the conventional RVG,  $V_{ref}$  is about 1.25V, and the  $V_{DD}$  minimum is 3.3V. However, in the proposed RVG, the operation voltage is simply limited by the resistance ratio of  $R_1$ ,  $R_2$ , and  $R_4$  and little influenced by the absolute value of the resistance. So the  $V_{DD}$  minimum varies with the temperature. Fig. 2 shows the measured  $V_{ref}$  characteristics of the proposed RVG.  $V_{ref}$  is 0.575V(at 27°C)  $\pm$  0.015V from -20°C to 100°C at 2.5V supply voltage.

The proposed VDC using the designed bandgap reference voltage generator depends on the matching of current mirror. However when the supply voltage is changed, current matching of a simple current mirror will be degraded. Wide-swing cascode current mirror can be used to improve the performance. Another effective method is to make use of amplifier.

The amplifier enforces the two inputs having equal voltage and PTAT current can be obtained. The operational principle is the same as the one using current mirror. However, the supply dependence is greatly reduced since the amplifier is able to enforce the two inputs to be equal at different supply voltages. Fig. 2 shows the measured  $V_{ref}$  characteristics of the proposed RVG at  $V_{DD}$ (at 2.375V, 2.5V, and 2.625V) variations.

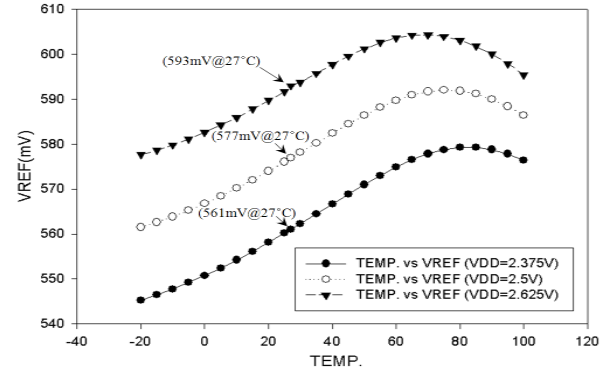


Fig. 2 Hspice result of  $V_{ref}$  voltage as a function of temperature at  $V_{DD}$  variations

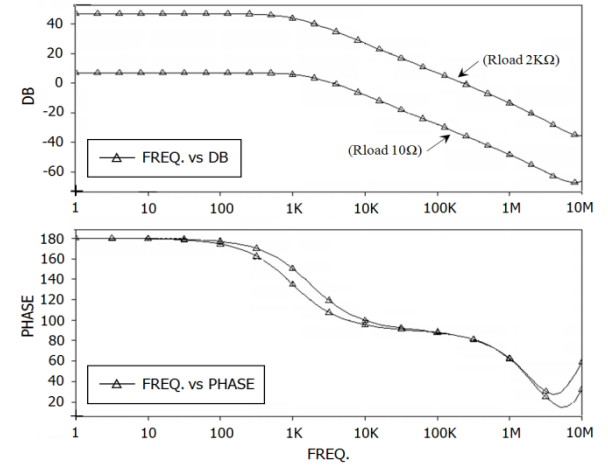


Fig. 3 Frequency response of the voltage-up converter

#### 3.2 Simulation results of VINT

The Voltage-up circuits should have enough current supply capability and a low output impedance so that the output voltage is not very much affected by the large loading current fluctuation. Fig. 3 shows the simulated gain and phase versus frequency for voltage-up with p-type pass transistor  $M_P$ . When the load impedance varies from 10 $\Omega$  to 2 k $\Omega$ ( $R_{load}$  from 100mA to 0.5mA), the phase margin is only among 60° to 90°, enough to ensure the loop stability for semiconductor device. Fig.4 is the simulation result of  $V_{INT}$  for different supply voltages, which can provide a stable voltage around 1.0V with external supply voltage of 2.5V. A capacitance  $C_{load}$ =20pF and resistance  $R_{load}$ =3 k $\Omega$  are used as the load impedance. Only  $\pm$ 0.12% deterioration of  $V_{INT}$  for  $\pm$ 5% variation of supply voltage  $V_{DD}$  is achieved. For temperature effects, the simulation results shown in Fig.5 indicate that the temperature dependency of  $V_{INT}$  is only 0.2mV/°C with the temperature ranging from -20 to 100°C. The simulation results shown in Fig.6 indicate that the proposed VDC can provide a maximum output current of 100mA when the output voltage  $V_{INT}$  is stabilized about 1.0V. Fig.6 shows the simulated result of  $V_{INT}$  for different load current.  $V_{INT}$  is among 1.0022V to 1.0044V when the load current changes from 0 to 100mA. Fig.7 shows the simulated transient response of the VDC. The output of the VDC can stabilize very quickly when the output impedance is varying. The transient response time is only 0.4  $\mu\text{s}$ .

Besides the pMOS pass device( $M_p$ ), the total current of VDC  $13.2 \mu A$ , which requires standby power dissipation of  $33.0 \mu W$ .

The output voltage( $V_{INT}$ ) is stabilized around 1.0V. Because the negative feedback in the voltage-up circuit can offer an adequate phase margin, and the output of the VDC will stabilize very quickly when the output impedance is varying. If a shorter transient response time is required, the voltage-up circuit should be biased at a higher current, which will take a larger power dissipation on standby mode of the VDC. Finally, the performance comparison of existing VDC is summarized in Table. 1.

Table 1. Performance comparison of proposed VDC

Key features list	[3]	[4]	Proposed
		5.0-3.3[V]	3.3-1.8[V]
Supply voltage variation vs. Output voltage[V]	3.295-3.305	1.774-1.801	0.985-1.015
Temperature variation vs. Output voltage[V]	3.265-3.355 (-40~100°C)	1.778-1.801 (0~70°C)	0.979-1.005 (-20~100°C)
Load current variation vs. Output voltage[V]	3.266-3.3 (0~100mA)	1.793-1.801 (0~100mA)	1.002-1.004 (0~100mA)
Transient response[ $\mu s$ ]	0.6		0.4
Standby power[ $\mu W$ ]	98.32	37.32	33.0

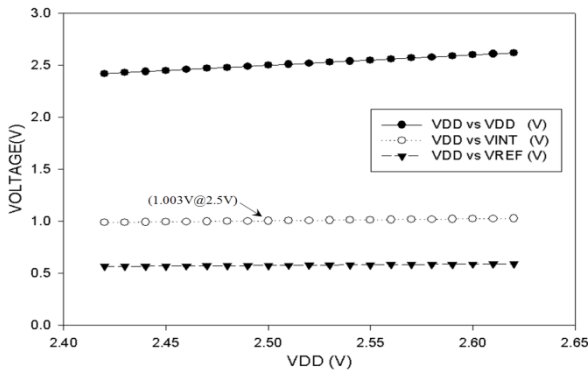


Fig. 4 Hspice result of  $V_{INT}$  and  $V_{REF}$  voltage as a function of  $V_{DD}$  variation

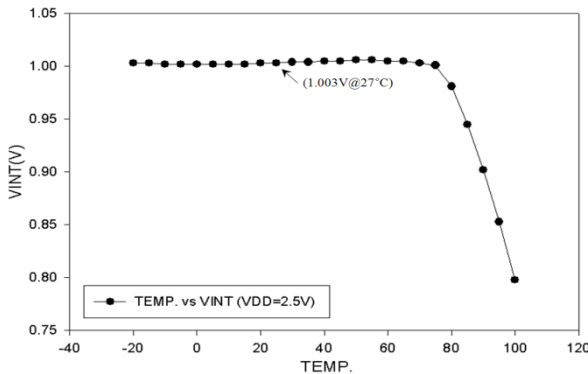


Fig. 5 Hspice result of  $V_{INT}$  voltage as a function of temperature

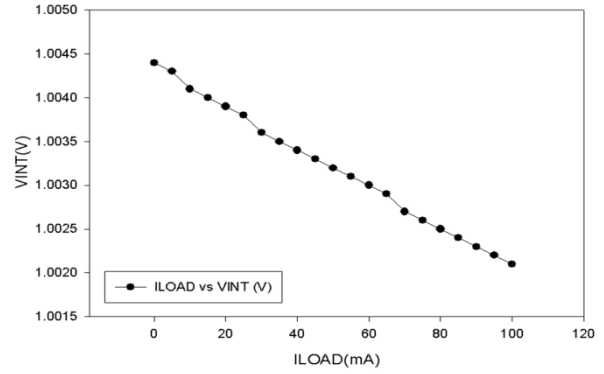


Fig. 6 Hspice result of  $V_{INT}$  as a function of output current

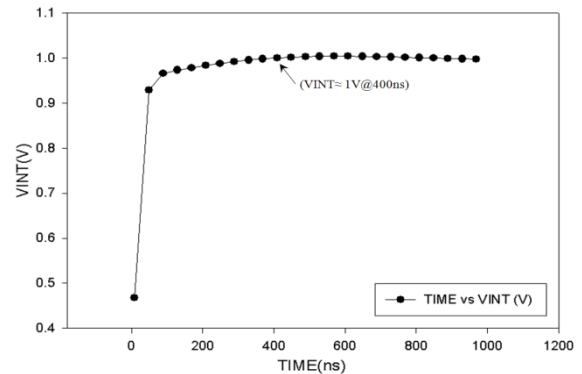


Fig. 7 The transient characteristic of the  $V_{INT}$

## 4. Conclusion

An on-chip VDC for analog and digital mixed circuit has been developed. It uses a negative-type voltage-up circuit with stability, relatively small temperature dependency, and small standby power dissipation. Therefore, it is well suited for low power IC chip. It converts 2.5V supply voltage to 1.0V in the internal supply voltage. In HSPICE simulation results, internal voltage is bounded (about 1.0V) in the proposed circuit when transient rapidly increases during  $0.4 \mu s$ . It has a couple of good characteristics such as low temperature dependency of only  $0.2mV/^\circ C$  and small voltage deviation within  $\pm 0.12\%$  for  $\pm 5\%$  variation of power supply voltage. This circuit is designed with a  $0.25 \mu m$  CMOS technology.

## References

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