A Design of 90 µW SENT Transmitter for Automotive Pressure Sensor in 0.18 µm CMOS Technology

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Abstract: In this paper, a low power and area efficient SENT transmitter design for automotive pressure sensor is proposed. The performance analysis and simulation results shows that the design is fully compliant with SAE J2716 standard. The proposed design is implemented using 0.18 µm CMOS technology with a very small active area of 116 × 116 µm² and it requires only 4.314 K gates. The current consumption is 50 µA from a 1.8 V supply and it requires only 90 µW power. The design is also synthesized for different FPGA families from Xilinx and Altera. The minimum occupied slice registers are 52 and maximum operating frequency of 595 MHz is achieved. The proposed design is also tested with a standard SENT receiver module and 100 % accuracy with zero error is verified.

1. Introduction

In automotive applications, large number of sensors report their information to the Engine Control Unit (ECU) [1]. For high resolution sensors, the conventional methods are no more suitable for such applications. The Single Edge Nibble Transmission (SENT) protocol is the emerging technique for high resolution data transmission in automotive industry. It is anticipated as a replacement for the lower resolution methods of 10-bit Analog to Digital Converters (ADC) and Pulse Width Modulation (PWM). It is a simple low cost alternative to Controller Area Network (CAN) or Local Interconnect Network (LIN) [2]. It is a unidirectional communication scheme from sensor to controller and does not require any synchronization signal from ECU. The sensor signal is transmitted as a series of pulses with data encoded as falling to falling edge periods. The synchronization/calibration pulse period is fixed which is followed by a status and communication, 1~6 data, Cyclic Redundancy Check (CRC) nibbles and optional pause pulse.

This paper focuses on the design of low power and area efficient SENT transmitter for automotive pressure sensor applications. The block diagram of pressure sensor Integrated Circuit (IC), incorporating the proposed SENT design is elaborated in Fig. 1. After gain adjustment, amplification, analog to digital conversion and essential processing, the pressure and temperature sensors data is applied to the input of SENT for transmission. The SENT module encodes the input data according to procedure defined in SAE J2716 standard and hands over it to ECU for monitoring and action.

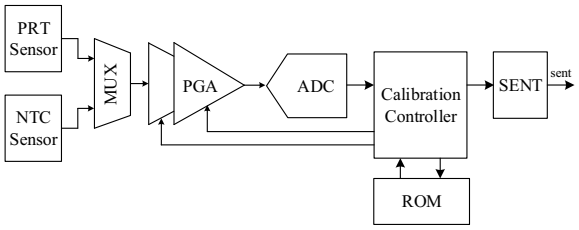


Figure 1. Pressure sensor block diagram

The rest of the paper is organized as follows: Section 2 presents the proposed design for SENT transmitter. The implementation and its results are summarized in Section 3. Finally, paper is concluded in Section 4.

2. Proposed SENT Design

The SENT architectural design is depicted in Fig. 2. Mainly, it is composed of Data Nibble Register (DNR), CRC Generator (CG), Pulse Encoder (PE) and SENT Controller (SC) modules. The DNR is a 24-bit parallel load shift register that loads and holds the input data nibbles from callibration controller for each SENT message sequence. During nibble pulses transmission, the register value is shifted left 4-bit at a time and most significant nibble is applied to PE. The CG block is responsible for calculating CRC from six registered input data nibbles according to the 4th order polynomial [1]. The internal architecture of CRC Generator is elaborated in Fig. 3. The PE sub-block along with multiplexer M1 generates the entire message sequence compliant to the SAE J2716. The SC monitors and schedules the activities of all other blocks. It generates control signals and observes the status of each block for generating message sequence. Figure 4 shows the flow chart for SENT transmitter. It has five states and is designed as Finite State Machine (FSM). Each state corresponds to exactly one part of the message sequence.

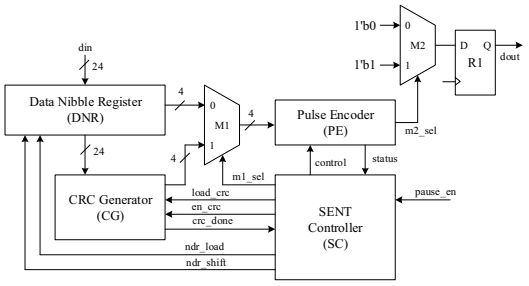


Figure 2. SENT transmitter architecture

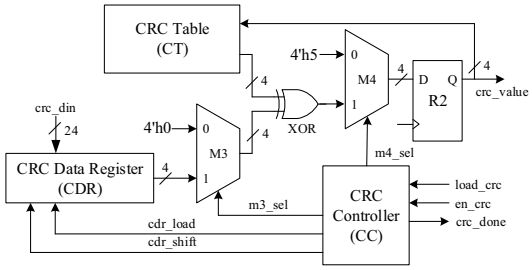


Figure 3. CRC generator architecture

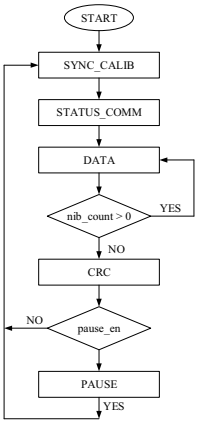


Figure 4. SENT Transmitter Flow Chart

3. Implementation and Simulation Results

The proposed design is implemented and integrated in a pressure sensor IC for automotive applications as shown in Fig. 1. The architecture is translated into circuit level by using Verilog HDL. For this implementation, the clock period is fixed to 8 µs and clock frequency is 125 kHz. The status and communication nibble value is fixed to zero and only fast channel is used with six data nibbles. If pause pulse is enabled, the constant message length is set to 282 clock ticks. In this case, the constant message duration is 2.256 msec. The design is implemented as datapath and control unit. The both SC and CC controllers are implemented as Moore state machine model using one hot state encoding scheme. This design is mapped using 0.18 µm CMOS technology with an active area of 116 µm × 116 µm. The selected chip layout pattern of pressure sensor ASIC focusing the SENT block is depicted in Fig. 5. It needs 4.314 K gates. The current consumption is 50 µA from a 1.8 V supply and it dissipates only 90 µW power.

The proposed design is also synthesized for various Xilinx and Altera FPGAs. The minimum occupied slice registers are 52 for Xilinx Artix-7 XC7A200T FPGA. The maximum operating frequency of 595 MHz is reported in case of Altera Stratix III EP3SE50F484C2 FPGA. Also the design is synthesized for Altera DE2-115 development board. It is tested extensively with KOPF Automotive Interface and KFlexExplorer for its verification. Figure 7 shows different simulation and implementation results. The Synopsys Design Compiler, IC Compiler and VCS tools are used for synthesis, place and route (P&R) and post-synthesis and post P&R simulations respectively. For functional simulation, Mentor Graphics tool ModelSim is utilized. The Cadence layout simulation is completed with HSPICE.

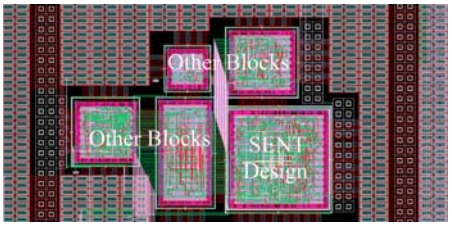
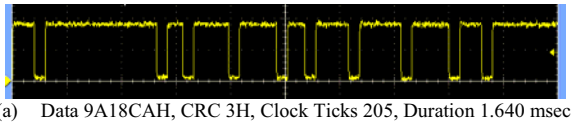
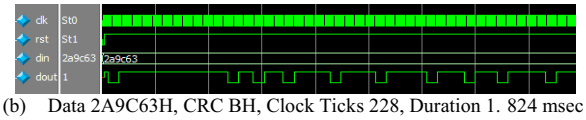


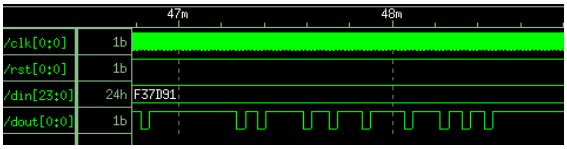
Figure 5. Chip Layout Pattern



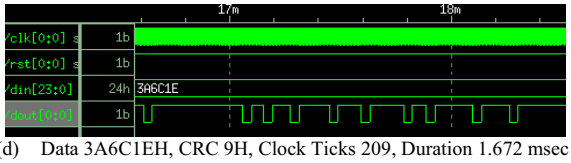
(a) Data 9A18CAH, CRC 3H, Clock Ticks 205, Duration 1.640 msec



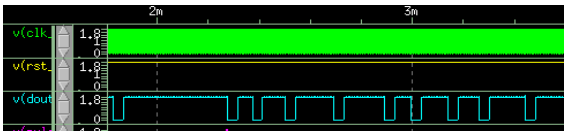
(b) Data 2A9C63H, CRC BH, Clock Ticks 228, Duration 1. 824 msec



(c) Data F37D91H, CRC 1H, Clock Ticks 201, Duration 1.068 msec



(d) Data 3A6C1EH, CRC 9H, Clock Ticks 209, Duration 1.672 msec



(e) Data 4CD163H, CRC BH, Clock Ticks 207, Duration 1.656 msec

Figure 6. Implementation and Simulation Results

4. Conclusion

This paper presents a low power and area efficient SENT design for automotive applications. The verification and simulation results prove that the design is fully compliant with the SAE J2716 standard. The proposed design is implemented using 0.18 µm CMOS technology with an active area of 13.456 mm² and it requires only 4.314 K gates. The current consumption is only 50 µA from a 1.8 V supply resulting 90 µW power requirements. As a result of synthesis for Xilinx and Altera FPGAs, minimum occupied slice registers are 52 for XC7A200T and in case of EP3SE50F484C2, maximum operating frequency of 595 MHz is reported. The SENT is also tested with KOPF Automotive Interface 4 and KFlexExplorer and 100 % accuracy with zero error is achieved. Low power consumption, small occupied area and high operational accuracy of the proposed SENT design make it very suitable for now a days automotive applications.

Acknowledgement

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References

[1] W. J. Fleming, "New Automotive Sensors—A Review", *IEEE Sensors Journal*, vol. 8, no. 11, pp. 1900-1921, Nov. 2008.

[2] J2716, "SENT – Single Edge Nibble Transmission for Automotive Applications", *SAE International*, Jan. 2010.