Relaxation Oscillator-Based Resistor Controlled Pulse Waveform Generator using Current Conveyors

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Abstract: A class AB current conveyor with low output impedance has been designed and simple square waveform geneators whose frequencies can be controlled by exteral resistor(s) also have been proposed. The current conveyor consists of class AB push-pull stage, complementary source-follower, and current mirror. The oscillator based waveform generators consist of two positive current conveyors (CCII+), two comparators, one RS-latch, two grounded capacitors and one(or two) resistors. The circuits are designed in 0.35um CMOS technology. Oscillating frequencies from 420kHz to 1200kHz were attained in the SPICE simulation. The waveform generators showed linearity error less than 2.5% and 3mW of power dissipation.

1. Introduction

After proposed by Sedra and Smith in 1970 [1], the CCII (also known as a current feedback amplifier: CFA) has been actively studied [2, 3]. Furthermore, it is well known that CCII is a useful building block in current-mode signal processing [4]. The CCII is composed of voltage follower between node X and Y, and current follower between node X and Z. As shown in fig. 1, it ideally features zero impedance at node X and infinite input and output inpedance at node Y and Z, respectively.

Recently, class A CMOS CCIIs considered for IC (Integrated Circuit) realization have been reported [5, 6]. These CCIIs feature their simple circuit configuration, small parasitic impedance and wideband voltage and current transfer characteristics. As will be described, small parasitic impedance at node X is essential to be used as a resistor controlled device. In order to meet this requirement, a class AB CCII has been designed by using local current feedback technique [7]. Furthermore, by employing the class AB stage, wider current input dynamic range and lower power dissipation have been achieved.

A square waveform generator is useful in the control of electromechanical systems and characteristics that can be controlled by external/internal components would be required depending on its application [8]. However, the previously reported pulse generator needs input pulse waveform to obtain output waveform. Therefore, in this paper, a class AB CCII with low current input impedance and its application to an oscillator based waveform generator are proposed. In section 2, the circuit configuration and operating principle of the proposed circuits are described and the proposed circuit performances are verified through SPICE simulation in section 3. Finally, we discuss two non-ideal effects on the circuits in section 4.

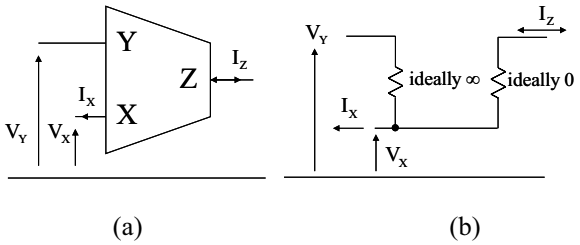


Fig. 1. (a) Block diagram and (b) its equivalent circuit of a current conveyor

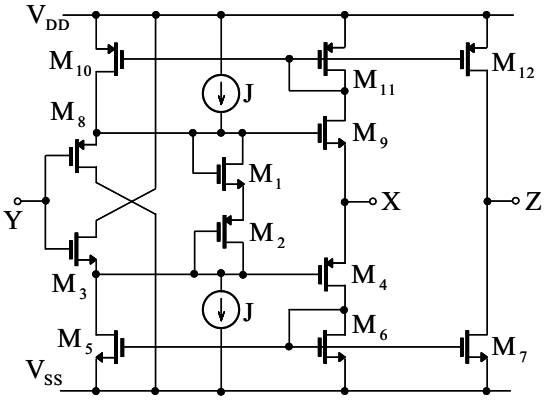


Fig. 2. Circuit diagram of the class AB current conveyor

2. Circuit configuration and operating principle

2.1 Design of a current conveyor

Fig. 2 shows the proposed CCII. In order to reduce the effect on load, it is essential that parasitic impedance at node X is as low as possible. By virtue of current mirror composed of M_5 and M_6, current flowing through M_6 is fed back to M_5 and this lowers voltage applied to the gate of M_4. Since the CCII is composed of complementary source-follower, the voltage applied to the gate of M_9 is lowered, too. Furthermore, this fact widens the input current dynamic range. The current current to M_5 controls voltage applied to the gate of M_4 as much as the input current variation at node X. By adopting the local current feedback technique and class AB stage, the parasitic impedance at node X is given by

$$r_x = \left(\frac{1}{g_{m9}} - \frac{1}{g_{m8}} + \frac{1}{g_{m9} g_{m11} r_{o9}} \right) \| \left(\frac{1}{g_{m4}} - \frac{1}{g_{m3}} + \frac{1}{g_{m4} g_{m6} r_{o4}} \right) \quad (1)$$

As shown in equation (1), the impedance can be regulated as low as ignorable by adjusting aspect ratios appropriately and, therefore, a condition for virtual ground is satsfied. In SPICE simulation the impedance have been measured approximately 25Ω, which is two times lower tha that of previously reported one. The bias current J was 50uA.

Because of the circuit configuration consisting of voltage follower, the input voltage at Y is conveyed to X. Considering the current feedback, the transfer function between the X and Y can de derived as

$$\frac{v_x}{v_y} = \frac{g_{m3} g_{m4} R_X}{g_{m3} - g_{m4} + g_{m3} g_{m4} R_X} \quad (2)$$

Where, R_X is external resistor connected between node X and ground. The transfer function can be controlled close to unity by adjusting aspect ratios. Output impedance of node Z can also be derived as

$$r_z = \left(g_{m12} r_{o12} \right) \| \left(g_{m7} r_{o7} \right) \quad (3)$$

Therefore, a matrix for transfer characteristics of the current conveyor shown in fig. 1 is satisfied as follows.

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0\ 0\ 0 \\ 1\ 0\ 0 \\ 0\ 1\ 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \quad (4)$$

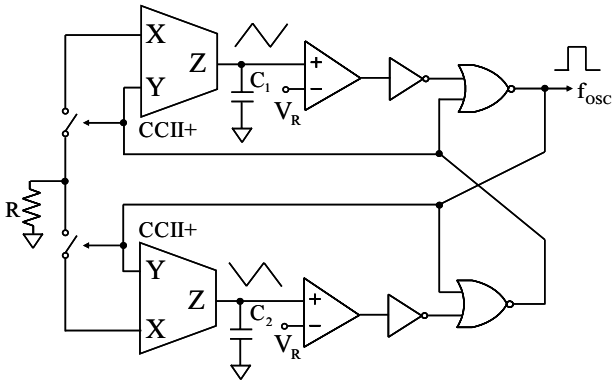
The simulated specifications on the CCII are summarized and arranged in table 1.

2.2 Design of an waveform generator

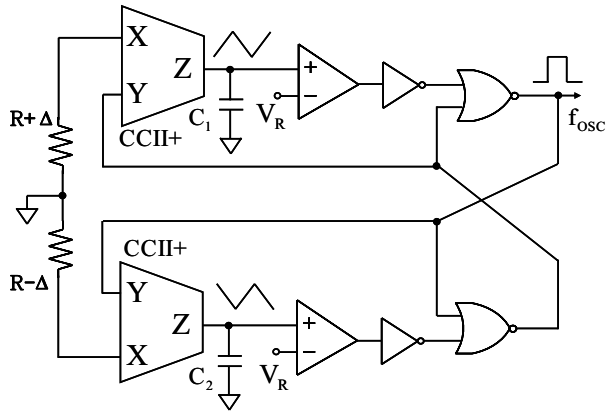
The proposed waveform generators and their waveform characteristics are shown in fig. 3 and 4, respectively. As described above, the CCII consists of voltage and current follower. Therefore, the CCII generates current inversely proportional to resistance value, and then conveys the current to the capacitor through the current follower. Since circuit configuration of the CCII is complementary, the capacitors are not charged simultaneously if we set the transistor size the same. The half cycle of the waveform is given by

$$t_1 = \frac{C}{I_{REF}} \left(V_{DD} - V_R \right) = -t_2 \quad (5)$$

If we take the absolute value for each width and sum up, the frequency of the single resistor controlled waveform generator can be written as



(a)



(b)

Fig. 3. Block diagram of the (a) single and (b) dual resistor controlled square waveform generator

$$f_{OSC} = \frac{I_{REF}}{C_1 + C_2} \cdot \frac{1}{V_{DD} - V_R} \quad (6)$$

Where I_{REF} is the mirrored current flowing through the transistor M_{12} and M_7 varied by the voltage applied to node Y and the resistor connected to node X. Considering capacitor charge and discharge time, the I_{REF} can be divided into two possible cases as shown in equation (7).

$$\begin{aligned} I_{REF} &= \frac{V_{DD} - V_{SD10} - V_{th9}}{R} \quad (\text{charge}) \\ I_{REF} &= \frac{-\left(V_{SS} - V_{DS5} - V_{th4} \right)}{R} \quad (\text{discharge}) \end{aligned} \quad (7)$$

Therefore, the final oscillating frequency can be written as

$$f_{OSC} = \frac{\left(V_{DD} - V_{SS} - V_{SD10} - V_{DS5} - V_{th9} + V_{th4} \right)}{2R \left(V_{DD} - V_R \right) \left(C_1 + C_2 \right)} \quad (8)$$

The voltage applied to node Y is generated by the RS-latch. Since output signals of the RS-latch are different each other, we can know that the resistor cannot be connected to the node X of both CCIIs at the same time. Similarly to the first

case, the each pulse width of the dual resistor controlled waveform generator is given by

$$t_1 = \frac{C_1(V_{DD} - V_R)(R + \Delta)}{V_{DD} - V_{SS} - V_{SD10} + V_{DS5} - V_{th9} + V_{th4}} \quad (9)$$

$$t_2 = \frac{C_2(V_{DD} - V_R)(R - \Delta)}{V_{DD} - V_{SS} - V_{SD10} + V_{DS5} - V_{th9} + V_{th4}}$$

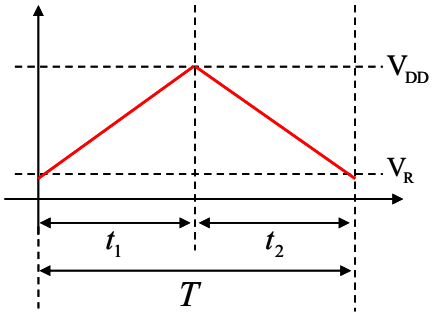


Fig. 4. Characteristic of voltage charged and discharged in the capacitors and its period

Simple one stage differential amplifiers have been used as a comparator to generate square waveform. In order to get rapid response time, however, two or three stage with high slew rate comparators can also be used. We set C=45pF, V_R=1.25V.

3. Simulation results

Simulation results on the proposed CCII and waveform generators are described in this section. The circuits are designed in SPECTRE by using CMOS 0.35um parameters.

Table 1. Simulated specifications of the CCII

	Specifications
Power supply	±2.5V
Power dissipation	1mW
Impedance at node X	25Ω
Impedance at node Y	∞Ω
Impedance at node Z	1MΩ
Voltage dynamic range	-0.75V ~ +1.25V
Current dynamic range	-300uA ~ +300uA
Unity gain bandwidth	4MHz

Fig. 5 shows the frequency of the generated pulse waveform as a function of single resistor. The oscillating frequency is in the range of 420~1200KHz and linearly depends on single resistor value. The resistor was varied from 8kΩ to 20kΩ.

Fig. 6(a) and 6(b) illustrate duty ratio of output waveform in case of dual resistor controlled waveform generator and its linearity error. These graphs show about 2% of offset error and up to 2.5% of linearity error. In this case, the resistors were changed within the range of -50kΩ to +50kΩ on center resistor 60kΩ. The generated waveforms in the simulation environment described above are shown in fig. 7.

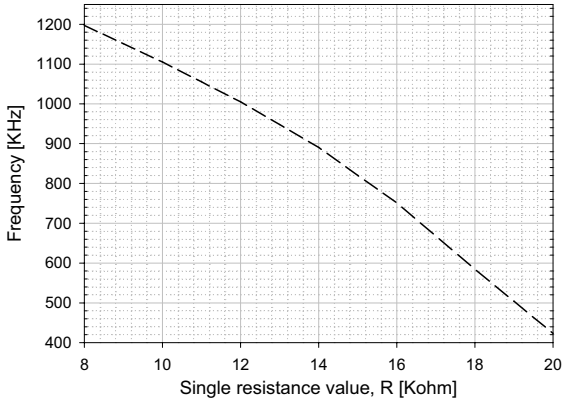
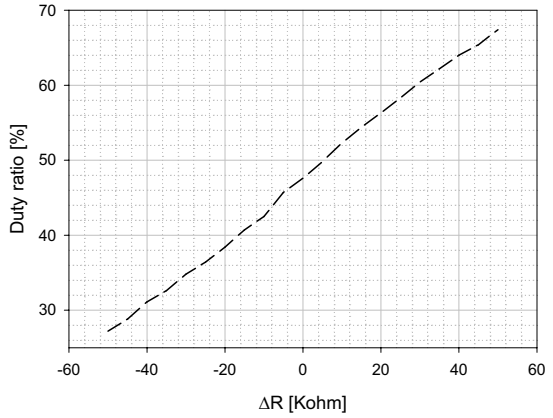
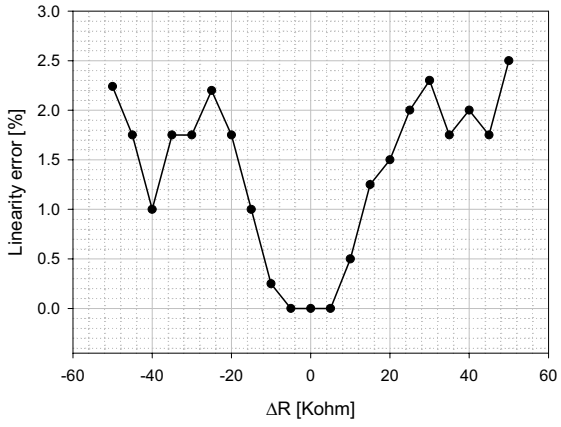


Fig. 5. The frequency characteristics of the pulse waveforms as a function of single resistor

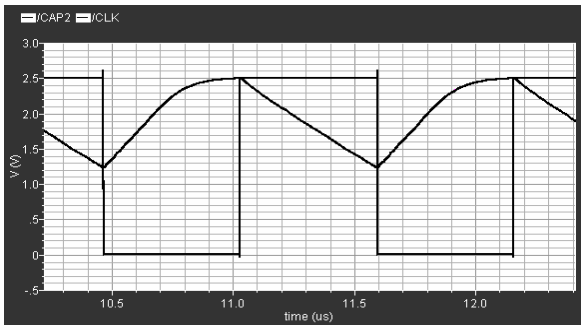


(a)

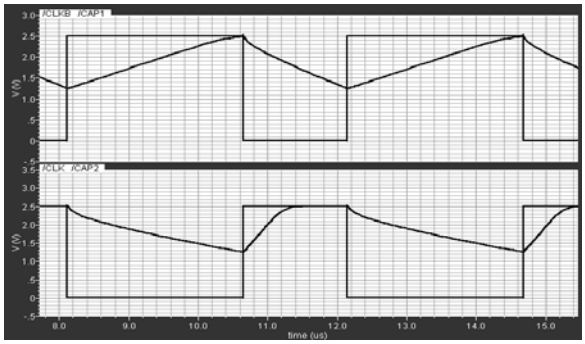


(b)

Fig. 6. The (a) duty raio as a function of dual resistor and (b) its linearity error



(a)



(b)

Fig. 7. The generated waveforms for (a) the single resistor controlled case (R=14kΩ), and (b) dual resistor controlled case (R_1=20kΩ, R_2=100 kΩ)

4. Nonidealities

In this section we discuss the non-ideal effects on performances of the circuits. Voltage applied at node Y transfers to X through M_8, M_9, M_3, and M_4. However, there is a little difference between NMOS and PMOS threshold voltage. In 0.35um CMOS process, the difference has been measured approximately 100mV. This makes difficult to make the voltage transfer function between node Y and X and current transfer function between Y and Z unity. The linearity error is caused by this non-ideal effect.

When the voltage chaged in a capacitor is larger than reference voltage V_R, the comparator changes its output state rapidly. However, due mainly to the limited slew rate of the comparator and propagation delay of logic gates, the generated pulses are delayed. This problem can be alleviated by using comparators with high slew rate and optimizing the aspect ratios of the logic gates.

5. Conclusion and future subjects

A class AB current conveyor with complementary source-follower and its application to a simple square waveform generator has been presented in this paper. Simulation results showed that the designed CCII has low parasitic input impedance compared to conventional one. Moreover, its application to oscillator based resistor-controlled pulse waveform generators has been verified through SPICE simulation. This indicates that the proposed circuit can be applied to a resistive sensor interface circuit. Furthermore, if we substitute two-element varying Wheatstone bridge for the single resistor as shown in fig. 3(b), this circuit can also be used as a resistance deviation-to-pulse width converter for simple micro-controller applications. The proposed circuits are under layout for sample chip fabrication.

6. Acknowledgement

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