

The Regularized FPGA Development Platform Verification Flow for Wireless Mobile SoC

Hyunil Kwon*, Jookwang Kim**, Sangmin Bae**, Kyungho Kim**, and Chungyong Lee*

* Dept. of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

**Modem R&D Team, Telecommunication R&D Center, Samsung Electronics Co., LTD., Suwon, Korea

Email : hikwon@csp.yonsei.ac.kr

Abstract - In the development and commercialization phase of information technology products implemented as a system on a chip (SoC), field-programmable gate array (FPGA) based platform has been widely used as the logic function test methodology for basic or advanced features and mobile station emulator. In this situation, to define the uniform verification approach on FPGA development platform, we introduce a regularized verification flow. To evaluate its availability, we consider 3rd generation partnership project (3GPP)-series Release 7 high speed packet access (HSPA) specifications. Finally along with this regularized verification flow, we have fully evaluated our implemented physical/higher layer of HSPA.

1. Introduction

The ever-increasing demands for high data rate and throughput in a mobile environment have led to SoC-embedded commercial products complying with various international standards. In this situation, to emulate the practical application-specific integrated circuit (ASIC) SoC, FPGA-based platform verification methodology has been used as the universal and inevitable approach.

To provide the regularized verification flow for FPGA platform, we consider 3GPP-series Release 7 HSPA among various wireless communication standards. HSPA is a collection of mobile telephony protocols that extend and improve the existing 3-generation universal mobile telecommunications system (UMTS) protocols. To be specific, HSPA is a combination of 3GPP Release 5 high speed downlink packet access (HSDPA), 3GPP Release 6 high speed uplink packet access (HSUPA) and other advanced features such as multi-input multi-output (MIMO) and continuous packet connectivity (CPC) etc. First HSDPA has additional transport/control channels over R99 UMTS such as high speed downlink shared channel (HS-DSCH) and three new physical channels (HS-SCCH, HS-DPCCH and HS-PDSCH). Also HSDPA has some features such as hybrid automatic repeat-request (HARQ) for an efficient retransmission of error-prone data, fast packet scheduling and adaptive modulation and coding for throughput enhancement and an efficient resource allocation. On the other hand, 3GPP Release 6 HSUPA has the enhanced uplink channels which extend the existing uplink channels with additional transport and control channels. The enhanced uplink channel will cater to the needs for mobile broadband communication with increased performance in the uplink, it will provide up to

5.8Mbps in the uplink, reduced delay and 150-200 percent greater system capacity [1][4][6].

To support 3GPP-series Release 7 HSPA functionalities previously stated, we introduce a regularized FPGA development platform verification flow for wireless mobile SoC. In addition to simple hardware operation based function test, a little complex operation based scenario test, interoperability test (IOT) connected with protocol stacks (layer 1 and layer 2/3) will be introduced. Also, we describe new test schemes for low power design, which is mainly applied to physical SoC.

This paper is organized as follows: section 2 describes the configuration of our platform. And section 3 explains the regularized function/scenario based verification and test flow to check the basic/advanced functionality. Finally conclusions are drawn in section 4.

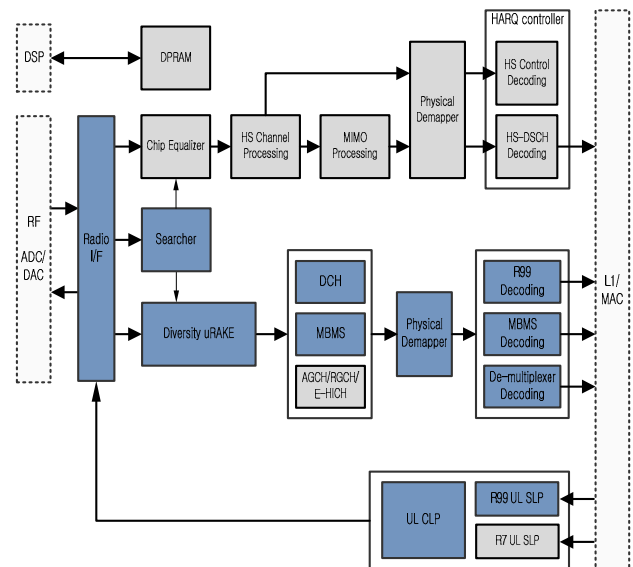


Figure 1: HSPA Block Diagram

2. Platform Configuration

Our developed platform consists of the modem engine for HSPA physical layer air-interface, the platform control engine embedding with an microcontroller (MCU) and a digital signal processor (DSP) core for protocol stack, and auxiliary functions for modem operation, and finally the peripheral engine for advanced testing.

A. Modem Engine

A HSPA modem engine having the structure shown on Figure 1 consists of radio interface block for radio frequency (RF) processing, searcher for pseudo-random noise (PN) timing acquisition, chip level processor, symbol level processor, de-multiplexer for channel decoding, uplink transmitter and timing controller. System specification for physical layer is shown in Table 1. Figure 2 shows the actual FPGA implementation.

Radio interfacing block performs automatic gain control (AGC), automatic frequency control (AFC) based on cross product frequency difference detector (CP-FDD), direct current (DC) offset correction for DC offset adjustment within the dynamic range, interpolation, square root raised cosine (SRRC) filtering and various RF interfaces for connection with commercial RF components.

Next searcher performs functions for initial cell search, re-acquisition, neighboring cell search, and multi-path search. Initial cell search is one for initial synchronization when user equipment (UE) is powered on. Re-acquisition compensates for the timing that is out of synchronization after waking up from sleep mode. Neighbor cell search operates for handover of UE located in cell boundary. Multi-path search finds multi-path delay profiles for rake/finger assignment. Also, offline search for power saving is supported.

Table 1: System Specification

Item	
Specification	3GPP Release 7 (HSPA)
	UMTS Terrestrial Radio Access Frequency Division Duplexing
	Wideband Code Division Multiple Access
	HSDPA/HSUPA
	Multimedia Broadcast Multicast Service CPC (Continuous Packet Connectivity)
Tx. Diversity	Space time transmitter diversity, Transmit adaptive array
Capability Class	Uplink/Downlink dedicated physical channel (384 kbps)
	Downlink high speed dedicated shared channel (28.8 Mbps)
	Uplink enhanced data channel (11.5 Mbps)
	Downlink capability w/ simultaneous high speed dedicated physical channel configuration (384 kbps)
	Uplink capability w/ simultaneous Enhanced-data channel configuration (64 kbps)
	Max bit rate for simultaneous HSDPA (28.8 Mbps)/HSUPA (11.5 Mbps)
RF	Power Class (Class 3)
	Freq. Band (Band I, II~X)

In hardware, the chip level processor consists of descrambler for primary/secondary scrambling code generator, secondary synchronization code generator, orthogonal variable spreading factor (OVSF) code generator for channelization, time tracker with delay lock loop for adjusting the rake/finger timing to track the arrival of an incoming

signal, channel estimator, interference signal code power measurement, and receive diversity processor based on pilot weighted combining (PWC), maximal ratio combining (MRC) and minimum mean-square error combining (MMSEC).

The symbol level processor consists of rake/combiner for diversity path combining, indicator detector for acquisition indicator channel (AICH), paging indicator channel (PICH), space time transmitter diversity (STTD) encoding detection, power control for closed and open loop power control unit to support various power control schemes, and physical layer measurement unit for channel condition check using parameters, such as received signal code power (RSCP), received signal strength indication (RSSI), time difference, etc.

The demultiplexer for channel decoding performs rate matching, 1st and 2nd de-interleaving, transport format combination indicator decoding containing information about transport channel (TrCH) combination, and channel decoding such as viterbi and turbo decoding.

Uplink transmitter performs the encoding chain for viterbi and turbo encoding, rate matching, and interleaving, the modulator chain for spreading, symbol mapping/gain scaling, scrambling and code generator, the timing generator for uplink channel transmission timing control, and discontinuous transmission scheme for power saving.

The timing controller manages receive/transmit data path timing based on the timing of multi-path rake/finger and cell information. It has system frame number (SFN) counter to support multiple cells and generates data path timing for each cell. For the timing of each cell, it provides frame boundaries and symbol clocks for combining path and channel decoder, and gives the reference frame signal to transmit for uplink data path. For the reference, the timing difference between downlink (DL) and uplink (UL) at the air interface should be within the specified range to make the base station recognize the uplink frame boundary.

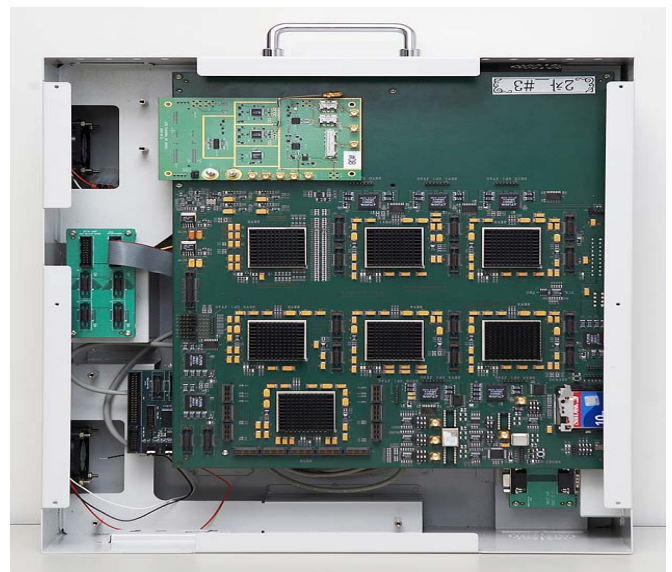


Figure 2: The implemented FPGA modem engine for HSPA

B. Platform Control Engine

This engine is implemented with MCU/DSP-embedded board and supports the interoperability of physical layer function units. Essentially, the modem engine is controlled by layer 1 software operating on MCU or DSP processor. As an effort to reduce MCU load, DSP performs additional functions to support advanced features such as equalizer and MIMO related processing. While, this platform interfaces are compatible with commercial ARM emulation board. On the other hand data transfer between MCU and DSP core is executed through dual port RAM or bus switching.

C. Peripheral Engines

This peripheral engine consists of data acquisition generation (DAG) board for physical layer function vector evaluation which is similar to Agilent ESG vector signal generator and DSP-embedded voice coder board for call test, which supports a variable rate code excited linear prediction (VR-CELP) for adaptive multi rate (AMR), which supports eight codec modes such as 12.2kbit/s, 10.2kbit/s, 7.95kbit/s, 7.4kbit/s, 6.7kbit/s, 5.9kbit/s, 5.15kbit/s, and 4.75kbit/s.

3. The Regularized FPGA Development Platform Verification Flow

The regularized FPGA platform verification flow consists of function test for simple command configurations and modem function evaluation, scenario test for complex command combinations and scenario based modem operation check, interoperation test with base station emulator, and physical chip emulation test for low power design. As a matter of convenience, we restrict the scope of discussion to WCDMA (R99) specification, which is a subset of HSPA.

A. Function Test

Before starting function test, as hardware-dedicated test, FPGA pin connection or mapping within each engines and various signals level validation should be carefully checked, especially clocks and some critical control signals.

Function test of the proposed flow is a three-step procedure. The first step is register read/write test in modem engine and some interrupt test for register setting are executed.

To evaluate each block's function in modem engine, known input vectors are used in the second step. That is, the output dump files using known input stimulus and the expected result files generated from the c-language link or simulator are bit-by-bit compared to check a normal operation of modem functions. The third one is mainly for various channel combinations, specific channel-dedicated features, and simple operation procedures. This step is frequently overlapped with the lower part of scenario test and handed over the scenario test. The detailed list for function test is categorized into the followings:

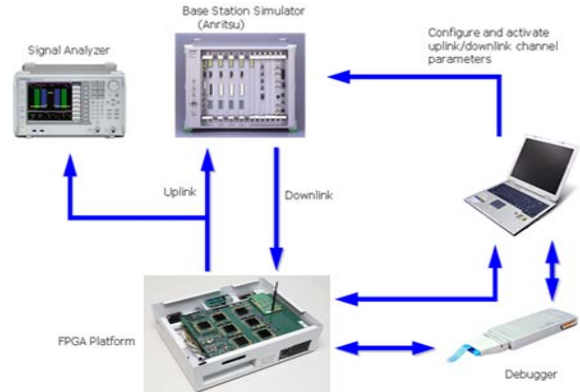


Figure 3: HSPA Platform Configuration for scenario test

- Register read/write test
- Interrupt test
- Modem function test
- Inter-RAT (Radio Access Technology) test
- RF test
- DRX (Discontinuous Reception) test
- Ciphering test

B. Scenario Test

This test is for the evaluation of physical and higher layer with a complex combination of physical channels as follow-up measures of function test. That is, along with implemented hardware functions shown on Figure 3, the following items are performed on protocol stack (layer 1 & layer 2/3):

- Cell search and broadcasting channel (BCH) decoding: After receiving the downlink cell synchronization command from the higher layer, this finds the BS having the biggest RSSI value among candidate BSs, executes 3-step search procedure, does BCH decoding procedure to find BS system frame number and check cyclic redundancy check (CRC) value.
- Random access channel (RACH) procedure: After receiving the RACH start command from the higher layer, this transmits RACH preamble in uplink, receives acquisition indicator channel in downlink, and transmits RACH message in uplink, demodulates message at BS, and finally checks CRC value.
- Compressed mode (CM): After receiving the CM-related command from the higher layer, MS and BS emulator pair checks each compressed mode packet's CRC value.
- UL/DL packet 384kbps: After receiving the related-command from the higher layer, mobile station and base station emulator pair checks each 384kbps packet's CRC value.
- Power control: After receiving the power control related-command including power up/down, this checks the power level's increase/decrease status through signal analyzer.

C. IOT with BS emulator

For cellular based applications, FPGA platform emulating mobile station should be tested with commercialized base station equipments or its emulator before commercialization. Call test with the complex setup procedure is appropriate for this application. To emulate these things, we consider the Anritsu equipment as BS emulator.

The overall test system for hardware/software interoperability consists of 2 notebook computers, Anritsu equipment, and FPGA-based platform. Figure 4 shows software flow in call test system including protocol stacks. And Figure 5 indicates test environment for WCDMA/R99 measurement and performance estimation.

Note-PCs are used for software downloading and monitoring, one mainly for FLASH, the other for DSP debugger, and Anritsu equipment, the signaling / protocol tester for the emulation of the base station functionalities including node-B and radio network controller. Signaling message exchanges and data transfers between FPGA-based platform and Anritsu equipment are performed through RF cable for simplicity. The PC used for flash download also displays the current call flow status in real time basis. With this configuration, voice call test for 12.2kbps AMR speech is successfully performed. Call set-up procedure between FPGA-based platform and Anritsu equipment is done in compliance with 3GPP signaling protocol specifications for layer1 and layer 2/3. Full voice call service software modules are implemented in this UMTS UE modem software.

D. Physical chip emulation test for low power design

Low power design for wireless mobile SoC to prevent power dissipation is a vital question. In terms of physical chip development stage, a well known solution for low power is clock gating. In this case, as alternative test methodology on FPGA platform, we consider the gated clock which based on power saving scenarios. And we again execute the existing function test on FPGA platform using the gated clock instead of the original clock source. Finally we can emulate the clock gating in physical ASIC process and simply validate the actual operation of clock gating cell. Meanwhile for an advanced testing, gated clock should be individually generated by each pre-defined clock domains and dynamically controlled by the actual operating scenarios on physical layers.

4. Conclusions

The regularized FPGA-based platform of wireless modem SoC complying with the mandatory of the 3GPP Release 7 HSPA specification has been implemented and evaluated in the following procedure: function test, scenario test, interoperability test and physical chip emulation test. Along with the proposed verification flow, we have evaluated the implemented physical layer and its interoperability with higher layer. Finally the proposed platform verification flow can be easily applied to any type of FPGA platform verification flow for wireless mobile SoC applications in the regularized manner.

References

1. Harri Holma and Antti Toskala, *WCDMA for UMTS: HSPA Evolution and LTE*, John Wiley & Sons, 2007
2. Andrew Richardson, *WCDMA Design Handbook*, Cambridge University Press, 2005
3. John A. C. Bingham, *The Theory and Practice of Modem Design*, Wiley-Interscience, 1988
4. 3GPP Rel. 7, "TS 25.101 - User Equipment(UE) radio transmission and reception (FDD)"
5. 3GPP Rel. 7, "TS 25.133 - Requirements for support of radio resource management (FDD)"
6. 3GPP Rel. 7, "TS 25.211 - Physical Channels and Mapping of Transport Channel onto Physical Channel (FDD)"
7. 3GPP Rel. 7, TS 25.212, "Multiplexing and Channel Coding (FDD)"
8. 3GPP Rel. 7, TS 25.213, "Spreading and modulation (FDD)"
9. 3GPP Rel. 7, TS 25.214, "Physical Layer Procedures (FDD)"
10. 3GPP Rel. 7, TR 34.108, "Common Test Environment for UE Conformance Testing"

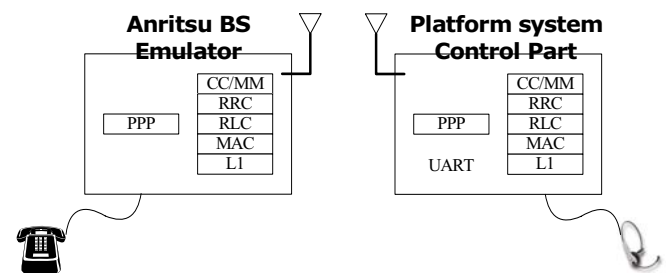


Figure 4: HSPA Software flow for Call Setup

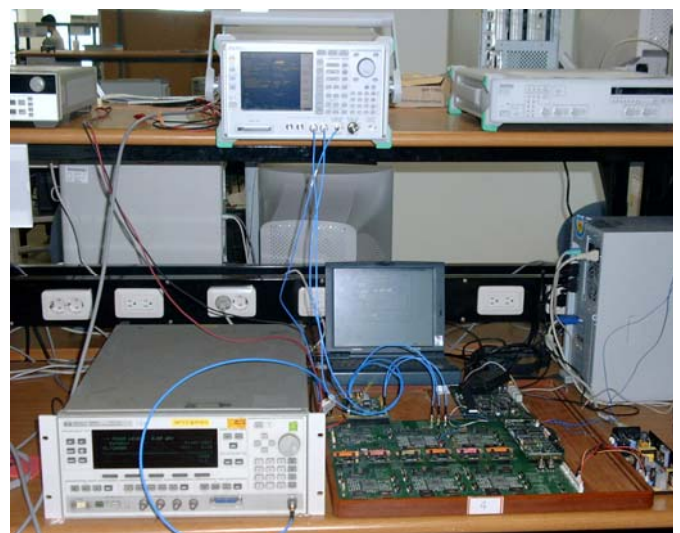


Figure 5: Test Environment for WCDMA/R99 measurement and performance estimation