Design of Clock Gears for Low-power Media Bus

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Abstract: In this paper, we design and verify a clock gear for low-power media bus. An audio applications use various sample rates i.e. 4K family (4, 8, 16, 24, 32, 48, 96 KHz) and 11.025K family (11.025, 22.05, 44.1, 88.2 KHz) frequencies. To support those frequencies, many clock sources are required and the fixed frequency of clock source often results in unnecessary power dissipation. Clock gears can simplify the problem related to clock. There is no need to use many clock sources but only one clock source can generate various clock frequencies. Clock gears can dynamically change the frequency of clock according to the amount of data for optimal power consumption. The Clock gear is designed in Verilog HDL and simulated. During simulation, the frequency of clock is calculated and automatically checked by a result verification program to validate the function of the clock gears

1. Introduction

For the mobile devices, multimedia functions such as MP3, DMB and video-conferencing are more important with appearance of the 3G phone. As the mobile device is required to integrate such multimedia functions with various and huge amounts of data, it needs much CPU time and consumes much power. In the mobile environment where only a limited power source e.g. battery is available, the power consumption is a significant problem.[1]
For the audio systems, besides speakers or headphones, codec for audio data also needs complex CPU computations and power. Because of the requirement to record and play back audio files at different sample rates, the CPU should convert the frequency. The conversion leads to slowing down the CPU and much power consumption.
In this paper, we propose and design a scheme to generate various audio frequencies with the use of single root frequency. The frequency of clock can be changed dynamically to reduce the power consumption.

2. MIPI SLIM Bus & Clock Gear

2.1 MIPI SLIM Bus

The Serial Low-power Inter-chip Media Bus (SLIMbus) is a standard interface between chips in mobile terminals and was developed within the MIPI Alliance[2]. SLIMbus supports for multiple high quality audio channels and peer-to-peer data communications. It is implemented by synchronous 2-wire, Time Division Multiplexed (TDM) frame structure.

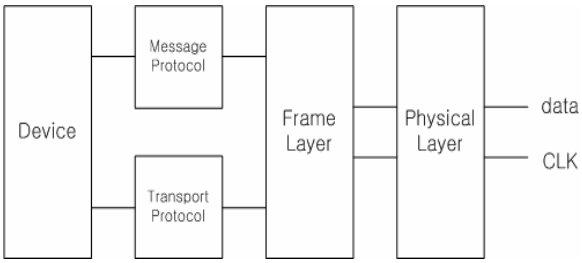

Figure 1. Simple SLIMbus component

Figure 1 illustrates the block diagram of a simple SLIMbus component. The Device is a logical implementation of a system function such as audio input or output. The Frame Layer combines control and data information into a bit stream. Also, it is used to split the bit stream into separate control and data streams. The Physical Layer provides for the transmission and reception of the SLIMbus bit stream between components. Data and control information sent from a Device are first encoded by specific protocols, the Message Protocol and the Transport Protocol.
For the communication in Physical Layer, two wires, CLK and Data are used. The CLK line is

not encoded but the DATA line is encoded using NRZI coding. Figure 2 shows the CLK and Data signals and the associated NRZI encoding. In this encoding, Data signal toggles when the value of real data is high. The Data and CLK lines are attached to two or more SLIMbus Devices to share the SLIMbus effectively. The multi-drop feature makes the SLIMbus useful to reduce the number of lines and power consumption.

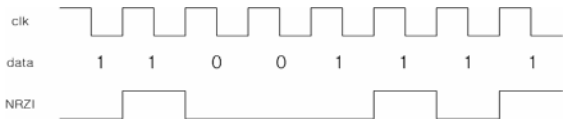

Figure 2. CLK and Data signal through NRZI encoding

2.2 Clock Gear

The Root Frequency of SLIMbus indicates the frequency of the CLK line as if the bus were in Gear 10. The Root Frequency may be changed while the bus is active while leaving the Frame Structure unchanged. A Natural Frequency is defined as a CLK frequency that allows a family of data rates to be supported. The different sample rate flows can be optimally supported by changing a particular Natural Frequency using the Clock Gear.

The bit stream rate can be changed while the bus is active by changing the Clock Gear. Clock Gears provide a range of power-of-2 frequency steps to operate SLIMbus.

$$\text{Rootfrequency} = \text{CLK\_frequency} \times 2^{(10-G)}$$

Table 1. The frequency for 4k family

Clock Gear	Natural Frequency (MHz) as a Function of Presence Rate							
	4k	8k	16k	32k	64k	128k	256k	512k
10	24.576	24.576	24.576	24.576	24.576	24.576	24.576	24.576
		16.384	16.384	16.384	16.384	16.384	16.384	16.384
9	12.288	12.288	12.288	12.288	12.288	12.288	12.288	12.288
	8.192	8.192	8.192	8.192	8.192	8.192	8.192	8.192
8	6.144	6.144	6.144	6.144	6.144	6.144	6.144	6.144
	4.096	4.096	4.096	4.096	4.096	4.096	4.096	4.096
7	3.072	3.072	3.072	3.072	3.072	3.072	3.072	-
	2.048	2.048	2.048	2.048	2.048	2.048	2.048	
6	1.536	1.536	1.536	1.536	1.536	1.536	-	-
	1.024	1.024	1.024	1.024	1.024	1.024		
5	0.768	0.768	0.768	0.768	0.768	-	-	-
	0.512	0.512	0.512	0.512	0.512			
4	0.384	0.384	0.384	0.384	-	-	-	-
	0.256	0.256	0.256	0.256				
3	0.192	0.192	0.192	-	-	-	-	-
	0.128	0.128	0.128					
2	0.096	0.096	-	-	-	-	-	-
	0.064	0.064						
1	0.048	-	-	-	-	-	-	-
	0.032							

If the Clock Gears increase, CLK frequency of the SLIMbus is also increased. Table 1 shows frequencies across all Clock Gears for the 4k family of sampling rate at the 24.576 MHz for Root Frequency. The clock gear is changed through the Message exchange to allow scaling the bus power consumption according to the application.

The SLIMbus bit stream is organized in a Time Domain Multiplexed (TDM) configuration. This organization allows SLIMbus to carry control and data information as well as bus configuration information.

A Superframe is defined as eight contiguous Frames (1,536 Slots), as illustrated in Figure 3. First slot of Superframe is Frame sync Symbol and slot 96 of Superframe is Framing Information. The 32-bit Framing information is divided into 8 slots and 1 slot is composed of 4 bits. Each slot of the 32-bit Framing information is sent by the Device once per Superframe in eight consecutive frames.

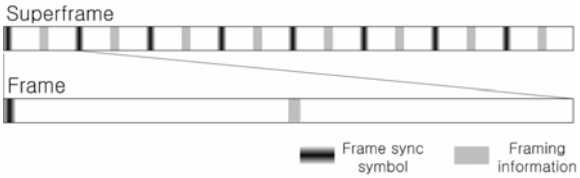

Figure 3. SLIMbus bit stream

Framing Information comprises of a flag for Framing Extension, fields for Subframe Mode, Clock gear and Root Frequency. Figure 4 shows the location of Clock Gear information in the Framing Information.

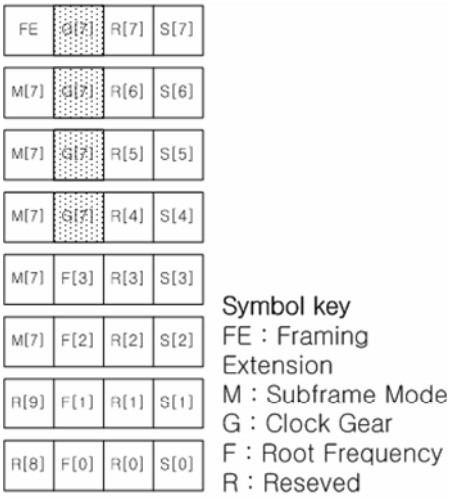

Figure 4. Framing information

The Clock Gear field, G [3:0], in the Framing Information shall be encoded as shown in Table 2. The root frequency can range from 12.8MHz to 28.8MHz. To obtain the required CLK frequency, the Clock Gear is dynamically set to suitable value according to the amount of application data.

Table 2. Clock gear coding

Coding (G[3:0])	Clock Gear	Minimum Frequency (MHz)	Maximum Frequency (MHz)
0000	Not Indicated	0	28.8
0001	1	0.025	0.05625
0010	2	0.05	0.1125
0011	3	0.1	0.225
0100	4	0.2	0.45
0101	5	0.4	0.9
0110	6	0.8	1.8
0111	7	1.6	3.6
1000	8	3.2	7.2
1001	9	6.4	14.4
1010	10	12.8	28.8
1011	Reserved	Reserved	reserved
1100			
1101			
1110			
1111			

The Root Frequency field, F [3:0], in the Framing information indicates the Root Frequency of the bus as coded in Table 3. The Root frequency ranges from 24.576MHz to 27MHz. By dividing this Root frequency, the required CLK frequency for most applications can be obtained.

Table 3. Root frequency.

F[3:0]	Root Frequency (MHz)	Phase Modulus (PM)
1111	reserved	reserved
1110		
1101		
1100		
1011		
1010		
1001	27	5625
1000	26	8125
0111	25	15625
0110	24	625
0101	19.2	125
0100	16.8	875
0011	15.36	100
0010	22.5792	147
0001	24.576	160
0000	Not Indicated	default

3. Design and Verification

3.1 NRZI coding and decoding

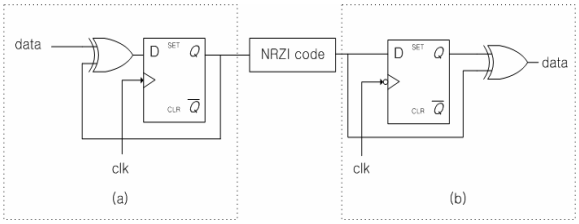

Figure 5. (a) NRZI encoder and (b) NRZI decoder

NRZI is one of the most frequently used coding schemes in the audio commutation.[3] In the NRZI encoder, if input data is high, output data toggles at the rising clock edge. But, if input data is low, output data remains unchanged. In the NRZI decoder, if input data transits at falling clock edge, the output data is high.

3.2 Framing information accumulation

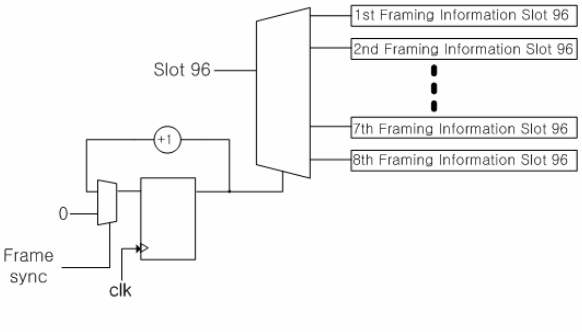

Figure 6. Framing Information

Superframe consists of eight frames. Frame has Message, Data, sync symbol and Framing Information. Frame information is divided into eight slots. Each information slot is inserted as the 96th slot from the sync symbol i.e. 1'b1011 in frame. As the sync symbol is sent in the first slot, the framing information slots is identified by a counter and merged to form the framing information. In the design, after the frame sync symbol is identified, the frame sync signal becomes active. Then, the counter starts increasing until it reaches to 96. At that time the 96th slot is collected and merged by the de-multiplexer. After all the slots are merged, the Clock Gear information is obtained.

3.3 Clock gear

Clock gear has 10 gear levels. Level 0 is the lowest possible number and level 10 is the highest. When the Clock gear is level 10, output clock frequency is same to the root frequency and the clock divider is not be used. Therefore, the root frequency passes by the clock divider as illustrated in Figure 7. Other clock frequencies at different Clock gear values except for 10 are generated through the clock divider. The increasing clock counter is compared with the Clock gear value. When the two values are same, the counter resets and the phase of the output clock is inverted so that the required clock frequency can be obtained.

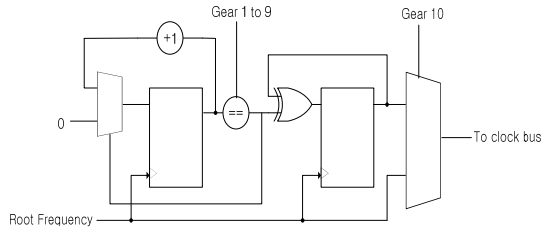

Figure 7. Clock Gear to generate the required frequency

3.4 Verification

The clock gear is designed in Verilog HDL and simulated. To verify the validity of the function, we wrote a program to check the clock frequency. The program generates test vectors that have stimulus for framing information, message and data. The clock frequency check program also recodes the time spans of the generated clock so that the result file can be compared to the expecting frequency file to determine a pass or fail.

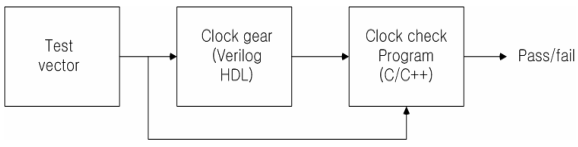

Figure 8. Scheme for hardware function verification

4. Conclusions

In this paper, we have designed Clock gear. Instead of always running the bus at the highest required frequency for a platform, Clock Gears can be used to tune the CLK frequency suitable for the current application and establish a framework for easily balancing bus band width. The Clock gear design was described in Verilog HDL and verified by the clock frequency check program.

Acknowledgment

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