# A Multimode CMOS Low Noise Amplifier Using Wideband Matching

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**Abstract:** This paper describes a 0.18 um CMOS wideband multimode LNA for wireless applications, such as WAVE (802.11p), WLAN (802.11a/b/g), WCDMA and Wibro. The circuit topology is a cascode structure with selective input path and wideband output matching for high gain with a low noise figure. By reducing the the quality factor (Q factor) of the narrowband LNA, it can get the flat passband gain. This structure is able to keep high gains in desired bands by adding a buffer. Simulation results show gains of 13.5 dB in 2 GHz and 13 ~ 15 dB over a bandwidth range from 3 to 5 GHz. This LNA achieves noise figures of 2.3 dB and 1.92~2.9 dB and power dissipations of 15.5 mW and 12.5 mW at 2 GHz and 3 ~ 5 GHz bands, under a power supply of 1.8V. The input/output return loss is less than -10 dB.

## 1. Introduction

Recently, wireless communication terminals have driven various applications, such as telephony, message and data transfer. These wireless devices have to be operated in multimode, covering multiple frequency bands and manifold standards. Therefore, the RF front-end must cover a wide range of different carrier frequencies for various standards. The simplest way is that each system has a separated input, however this is inefficient to be applied the portable devices. For overcoming these weak points, other ways such as wideband LNA and concurrent LNA are developed to receive signals that are applied to multi-standards. These ways indicate a high noise figure due to its difficulty to obtain a proper noise matching in the wide frequency range. That is to say, the LNA receiving the targeted signal among the various frequencies is able to have good noise efficiency by optimizing the input noise matching in each frequency.

In this paper, a multimode CMOS LNA, which can receive selectively signals of multi-standards, is presented. The wideband matching of output impedance and simultaneous input and noise matching of input impedance enable achieving a good performance in the wide frequency range. The wideband matching circuit can help the usage of the same component for the output impedance matching at the multi-band. Therefore, the proposed LNA that fulfills the requirement of WAVE (802.11p), WLAN (802.11a/b/g), WCDMA and Wibro has low noise figure and high gain characteristics.

## 2. Topology of the proposed Multimode LNA

The proposed LNA shown in Figure 1 adopts a cascode structure that has many advantages such as a great isolation between input and output, high gain, and decreased Miller effect [1]. It is operated in multi-band by selective input path and wideband matching.

Normally, LNA operating in wideband is difficult to represnt a good performance in low frequency band [2]. Hence, the method needs for a good efficiency in low frequency. Input of the proposed LNA have two paths in 2 GHz and 3 ~ 5 GHz. Input matching network of the LNA has two pathes that is selected by the $SW_1$ and the $SW_2$. When the $SW_1$ is turned on, it is operated in 2 GHz band. The $SW_2$ can be selected to run it in 3 ~ 5 GHz bands. Output matching network of the designed LNA enables the usage of the same components at the multi-bands and provides high gains at the operating frequencies. The designed LNA can improve the linearity and noise characteristics of circuits, in comparison with the output matching using switching components in desired frequency [3].

### 2. 1 Input and noise matching at low frequency

Figure 2 shows the small-signal equivalent circuit of the input network for the noise analysis. By turning on the $SW_1$, the input matching network, indicated by Figure 2, is optimized in 2.4 GHz. The input impedance ($Z_{i1}$) is expressed as

$$Z_{i1} = j\omega_1(L_1 + L_{s1}) + \frac{g_{m1}L_{s1}}{C_{gs1} + C_1} + \frac{1}{j\omega_1(C_{gs1} + C_1)} \quad (1)$$

where $g_{m1}$ is the transconductance of $M_1$ and $C_{gs1}$ is the capacitance between gate and source of $M_1$.

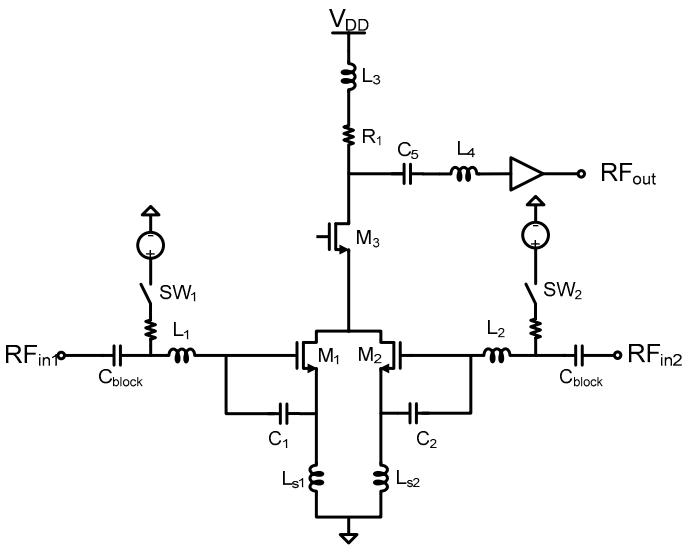


Figure 1. Schematic of the designed LNA

For the simultaneous input and noise matching, the input impedance condition should be satisfied

$$Z_{opt} = Z_{i1}^{*} \tag{2}$$

The optimum noise impedance ($Z_{opt}$) has to be determined for the minimum noise figure by selecting proper values of $L_1$, $L_{s1}$, W/L of $M_1$ and giving a suitable bias point. The degeneration inductor ($L_{s1}$), which is caused to achieve Equation (2), makes simultaneous input and noise matching to be possible without degradation of $F_{min}$ and $R_n$ [4].

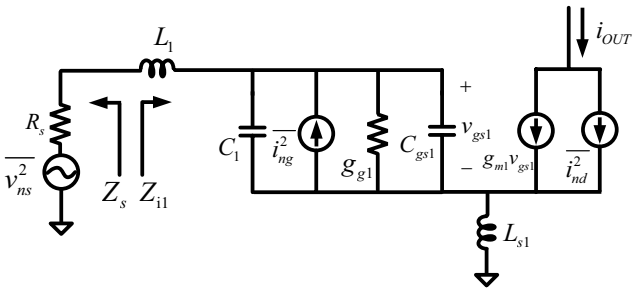


Figure 2. Small-signal equivalent circuit of input for 2 GHz band operation.

**2. 2 Wideband input and noise matching**

By turning on the $SW_2$, the LNA is able to be operated in 3 ~ 5 GHz. The input impedance of LNA is given by

$$Z_{i2} = j\omega_2(L_2 + L_{s2}) + \frac{g_{m2}L_{s2}}{C_{gs2} + C_2} + \frac{1}{j\omega_2(C_{gs2} + C_2)} \tag{3}$$

$\omega_2$ is the transit frequency. This input matching network is designed by simultaneous wideband input and noise matching. Though the structure is same as the circuit which is operated at 2 GHz, the design parameters are optimized for the 3 ~ 5GHz operation. In order to obtain this matching, the input source impedance, $Z_s$, seen from the gate of the input transistor should be the complex conjugate of $Z_{i2}$ and at the same time be equal to $Z_{opt}$. Im[$Z_{opt}$] is similar the form of the complex conjugate of Im[$Z_{i2}$] [4]. This is as follows

$$\mathrm{Im}[Z_{opt}] = -\omega_2 L_2 - \frac{K}{\omega_2(C_{gs2} + C_2)} \tag{4}$$

K is a dependant technology parameter. This value is close to 1, as technology scale is smaller. In addition, the effect of Im[$Z_{opt}$] and Im[$Z_{i2}$] disappears at high frequencies, further improving the matching. The matching of Re[$Z_{opt}$] and Re[$Z_{i2}$] is tougher in the wideband. This is because the former is frequency dependant, while the latter is constant and bias dependant. Because Re[$Z_{i2}$] also depends on the value of $L_{s2}$, it can be optimized the circuit for wideband LNA by suitable choice of this inductance.

**2. 3 Output matching**

For high gains at multi-band frequencies, the proposed LNA is optimized for wideband output matching. Primarily, the resonance frequency is designed for the narrow-band operation by using inductor and the quality factor (Q factor) of a shunt peaking inductor ($L_3$) should be as high as possible. This has a high-gain at only narrow-band. However, for having high and flat gains of LNA at multi-band, the Q factor of the shunt peaking inductor ($L_3$) in circuit should be kept smaller [5]. The output load of the designed LNA is composed of a RLC network. The impedance of the network is

$$\begin{aligned} Z(s) &= (sL_3 + R_1) // \left( \frac{1}{sC_{out}} + sL_4 \right) \\ &= \frac{s^3 L_3 L_4 C_{out} + s^2 R_1 L_4 C_{out} + sL_3 + R_1}{s^2 L_3 C_{out} + s^2 L_4 C_{out} + sC_{out} R_1 + 1} \end{aligned} \tag{5}$$

The ouput gain is $-g_{m1}/s(C_{gs1}+C_1)$ or $-g_{m2}/s(C_{gs2}+C_2)$ in an ideal operation. In the frequency band, the gain can be given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{s(C_{gs} + C_{ex})R_s} \cdot \frac{s^3 L_3 L_4 C_{out} + s^2 R_1 L_4 C_{out} + sL_3 + R_1}{s^2 L_3 C_{out} + s^2 L_4 C_{out} + sC_{out} R_1 + 1} \tag{6}$$

The shunt peaking inductor ($L_3$) is resonant with the total parastic capacitance ($C_{out}$) at the drain of $M_3$. The upper device ($M_3$) of cascode structure is chosen smaller to have less parasitic capacitance. Therefore, $R_1$ and $L_4$ is added to reduce the quality factor of the load to guarantee the channel bandwidth [6]. The series inductor ($L_4$) offers the flat gain in the high frequency. An upper limit to $L_3$ and $R_1$ is set by the size and the voltage headroom respectively. By doing a conjugate matching with a buffer in output, it can have a higher gain. It is composed of a simple common drain transistor witch offers a broadband gain. Figure 3 shows the schematic of the buffer, the output impedance is equal to $r_{o4}/(1+g_{m5}r_{o4})$ and the additional gain is

$$A_{vbuffer} = g_{m5} \cdot \frac{r_{o4}}{1 + g_{m5} r_{o4}} \tag{7}$$

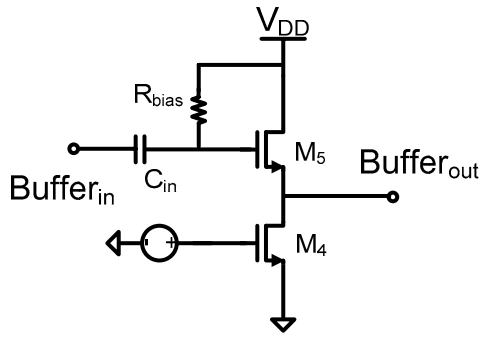


Figure 3. Small-signal equivalent circuit of input for 2 GHz band operation.

## 3. Simulation results of the designed LNA

A multimode LNA is designed in TSMC 0.18 um CMOS technology and simulated by RF spectre of cadence. A die photo of the LNA is shown in Figure 4 whose size is 920 um × 940 um. Except for the output blocking capacitors and degeneration inductors, all components are integrated on a single-chip. The input impedance of circuit is close to 50Ω in the each band. Due to the buffer, the output of circuit is well matched to 50Ω for measurement purposes. The total power consumptions at 2 GHz and 3 ~ 5 GHz bands are 15.5 mW and 12.5 mW, respectively. As shown in Figure 5, the input return losses in a each frequancy bands are less than -10 dB. The gains at 2 GHz and 3 ~ 5 GHz bands are 13.5 dB and 13 ~ 15 dB, respectively. The noise figures are revealed in the Figure 6. The noise figures are held about 2.3 dB and 1.92~2.9 dB in a each frequancy range, and IIPs of -7.4 dBm and -5 dBm are obtained in 2.4 GHz and 3 ~ 5 GHz, respectively.

The simulated results show that there is no significant performance degradation by a selective frequency band and wideband output matching network. The simulation results for the integrated multimode LNA are summarized in Table 1.

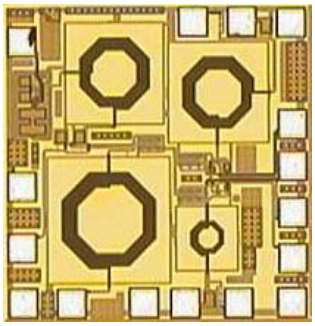

Figure 4. Die photo of the designed the multimode LNA

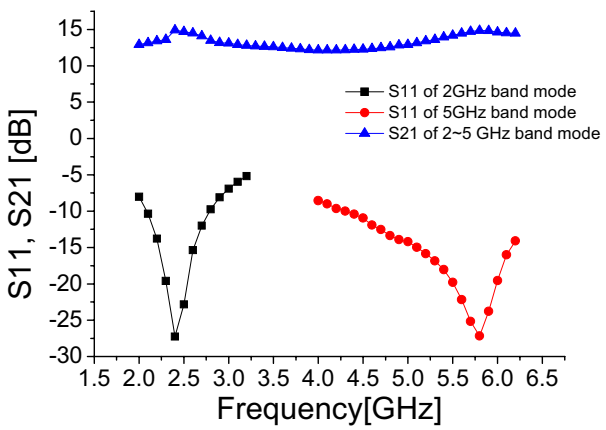


Figure 5. The input return loss and gain of multimode LNA

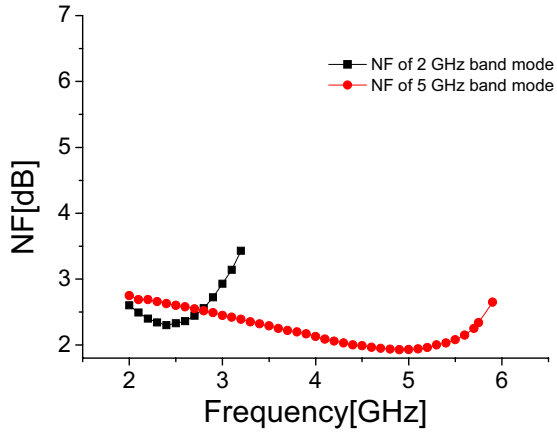


Figure 6. Noise figures at 2 GHz and 5 GHz bands operating condition

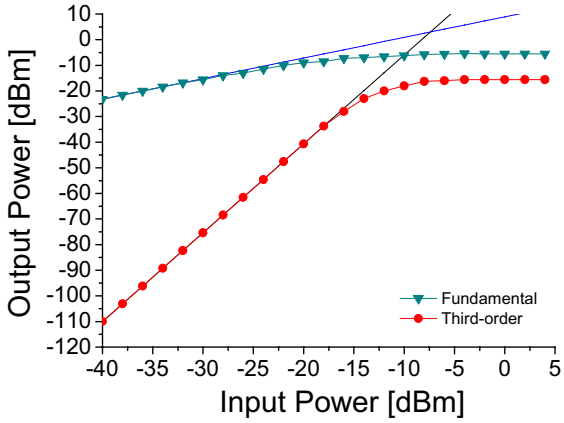


Figure 7. IIP3 at 2 GHz band

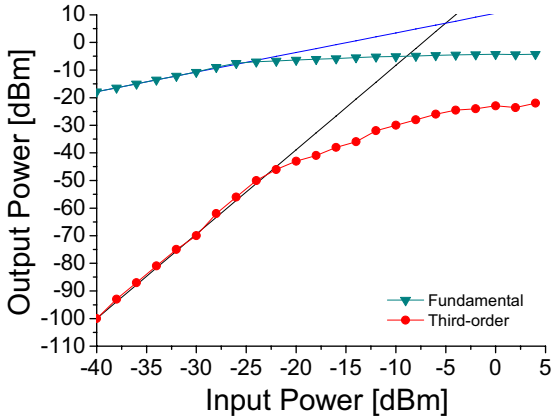


Figure 8. IIP3 at 3 ~ 5 GHz bands

## 4. Conclusion

The multimode LNA is implemented for WAVE (802.11p), WLAN (802.11a/b/g), WCDMA and Wibro applications in 0.18 um CMOS technology. A multimode LNA for the 2 GHz and 3 ~ 5 GHz operations with input path switch is proposed in this paper. By optimizing wideband matching, selecting input path and using the capacitor in parallel with the $C_{gs1}$ and $C_{gs2}$, the designed LNA acheives good noise figures and high gains at various applications. It results a 13.5 dB/13 ~ 15 dB gains and a 2.3 dB/1.92~2.9 dB noise figures at the 2 GHz and 3 ~ 5 GHz band, respectively.

Table 1. Performance summary of proposed LNA

| ***Frequency [GHz]*** | 2 | 3 ~ 5 |
|---|---|---|
| ***Gain [dB]*** | 13.5 | 13 ~ 15 |
| ***Noise Figure [dB]*** | 2.3 | 1.92 ~ 2.9 |
| ***IIP3[dBm]*** | -7.4 | -5 |
| ***Power Consumption[mW]*** | 15.5 | 12.5 |
| ***Supply Voltage[V]*** | 1.8 | |
| ***Technology*** | 0.18 um CMOS | |


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