Method of Comparator Offset Manipulation by Fowler-Nordheim Stress

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Abstract: In this paper, we propose a method to manipulate offsets of comparator circuits. By selective FN stressing on MOS transistors, it alters MOS threshold voltages and the comparator offset resultantly. This method has numerous advantages over the conventional offset cancelling methods, not increasing circuit area, nor degrading operation timings, nor demanding the floating gate process. This method also can be utilized for a read-only memory cell by intentionally implanting positive or negative offsets, which is multiple times programmable with the standard CMOS process. We apply it to the latch-type comparator and show that the offset get adjusted to the desired value through experiments.

1. Introduction

The comparator offset have been regarded as an uncontrollable parameter that has great influence on the circuit performance such as the bit resolution in an analog-to-digital converter. The offset originates from the process non-uniformity assuming the circuit design is completely symmetric. Any mismatches in device parameters between two differential counterparts bring about the offset.

A good deal of efforts has been done to eliminate the offset or effects of the offset [1-3], however they always require 'something additional' such as timing stage, increased layout, or floating gates, which seriously increases design or manufacturing costs.

We introduce a new method to manipulate the comparator offset through physical phenomena of the MOS transistor, i.e., the Fowler-Nordheim (FN) stress degradation. This method makes use of the nMOS and pMOS cross-coupled pair topologies of the comparator for the FN stressing on chosen MOS transistors. The cross-coupled topology is commonly employed for the positive feedback action in comparators, it is applicable to nearly every kind of CMOS comparator circuits.

Because this method uses an intrinsic property of CMOS device, this method does neither hurt circuit performance nor increase layout area. By manipulating comparator offset, we can derive a new concept of ROM memory as well as eliminate undesired offsets in VLSI circuits.

2. V_T Shift by FN Stress

The Fowler-Nordheim tunneling increases steeply as the vertical electric field intensity exceeds 8MV/cm in the gate oxide. The tunneling carrier can be captured in bulk oxide traps and the captured charge shifts the threshold voltage of MOS transistors. The tunneling carrier may also generate new interface trap in the Si-SiO_2 interface with high energy, which also raises the threshold voltage by degrading the subthreshold slope. In conclusion, MOS transistors become weaker in current drivability as it undergoes the FN stress condition. [4-5]

The FN tunneling current increases exonentially as the gate voltage increases. Therefore, the threshold voltage shift has an exponential relation to the gate voltage. And it also shifts linearly as the stress time proceeds to some extent. As more oxide traps become occupied, the threshold voltage shift becomes slow.

NMOS threshold voltages begin to move at a lower gate voltage than PMOS's. In the surface channel pMOS' case, it can be ascribed to the large electron affinity of the p+- poly gate. In the buried channel pMOS's case, it is due to the lower oxide field. [6] Fig. 1 shows measurement results of threshold voltage shifts by FN stresses for 0.35μm standard CMOS transistors. We can find that the threshold voltage shifts linearly until it reaches about 100mV and beomes slow after that in these devices.

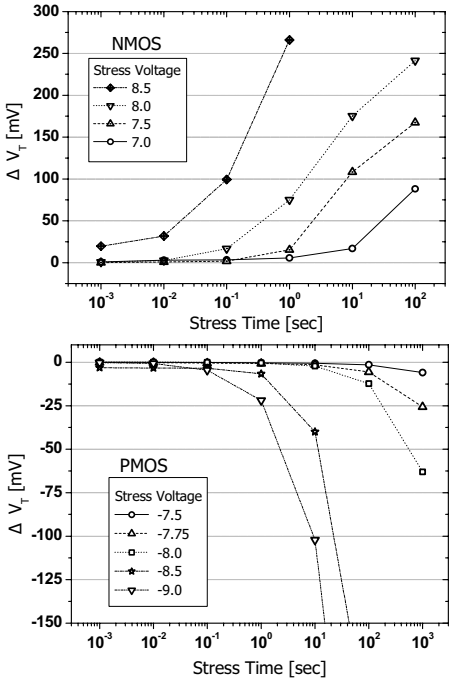

Fig.1 nMOS & pMOS V_T shifts according to FN stress voltages and stress times.

3. Comparator Offsets

CMOS comparator circuits compares two input voltages and produce digital level output voltages. The transfer curve of an ideal comparator has the trip point at the zero input voltage. However, the trip point shifts if the comparator has a non-zero offset value. The offset is usually modeled as an internal fixed noise voltage source in comparators. Fig. 2 shows transfer curves of real comparators with non-zero offsets. We can see that the sign of offset value corresponds to that of output value.

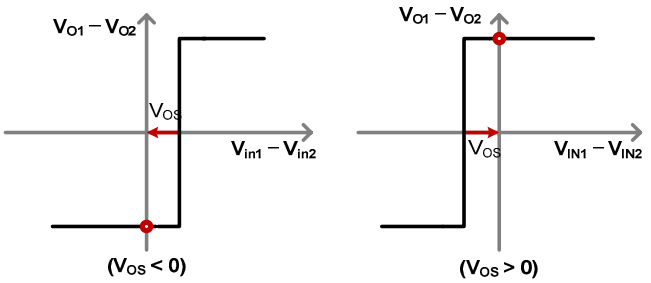

Fig. 2 Comparator transfer curves according to the sign of its offset

Comparators commonly use the positive mechanism for the abrupt transition in the transfer curve. The positive feedback is realized by the cross-coupled transitor pair topology. Fig. 3 shows one of the common comparator circuits which includes the cross-coupled pMOS and nMOS transistor pairs.

The latch-type comparator is a suitable test bed for the offset manipulation because it is the basic form among various comparators using the positive feedback. It comprises two cross-coupled pairs, the commonly demanded topology for positive feedback action in most comparator circuits. In practice, it is prevalently used as the bit-line sense amplifier in the dynamic random acess memory applications.

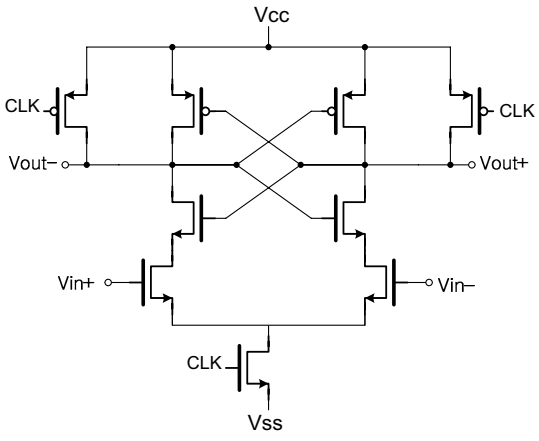

Fig. 3 A comparator circuit including the cross-coupled nMOS & pMOS transitor pairs.

The offset of comparator is caused by any kind of mismatches between the two differential parts including parasitic capacitance, contact resistance, channel mobility, etc. However, they can be converted into the equivalent threshold voltage mismatches between two counterpart transistors in that the threshold voltage difference is reflected to the offsets by unit scale.[7] Offsets of the latch-type comparators are substantially determined by one part whose common source node is enabled first, between the pull-up and the pull-down transistor-pairs

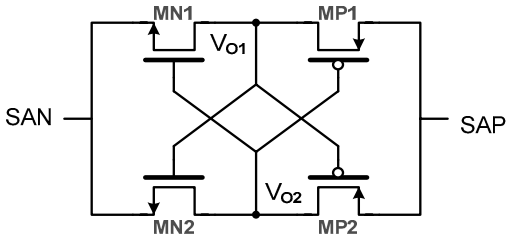

Fig. 4 The latch-type comparator circuit

4. Offset Manipulation Method

Considering the above described characteristics, we can see that we can manipulate the offset of comparator circuits by selective MOS transistor stressing. Let us look into the method eliminating the offset to zero first. As seen in Fig. 2, the output voltage at the zero input voltage is determined by the sign of the offset. Assuming the positive offset value in Fig. 4, (V_{O1}-V_{O2}) goes high when it is enabled, meaning V_{O1}=V_{CC} and V_{O2}=V_{SS}. If the SAP voltage is raised to the stressing voltage, so is the V_{O1} voltage. Then, MP1 and MN1 transistors enter the FN stress condition, which leads to increases in absolute threshold voltages. Raised thresholds in MP1 and MN1 result into a reduced comparator offset value.

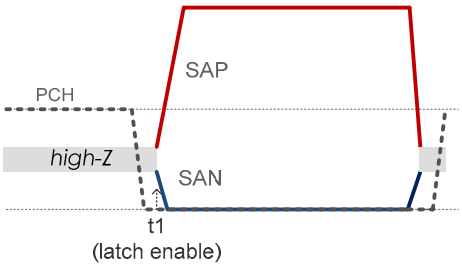

Fig. 5 The stress-packet signal timing plot

As this stress condition continues, however, the offset will reach zero and even go past it beyond. There is no way to detect the zero offset and to stop stressing just at it. Instead of the continuous stressing, we can use a ‘stress-packet’ method which repeats an offset-evaluation (precharge & enable) and short-time stressing (supply elevation) operations periodically. It will drive the offset to converge to zero by negative feedback mechanism. After reaching zero, the offset value begins to oscillate in zero’s vicinity. This method also enables simultaneous offset cancellation for numerous sense amplifiers, which is an important feature for practical applications to the DRAM and the flash-type ADC.

As well as eliminating offsets, it is also possible to set a desired offset value to a comparator in similar ways. Fig. 6

shows the mechanism that the comparator offset is driven to converge to the applied non-zero input voltage by performing stress-packets. We have explained that FN stressing under high VO1-VO2 condition forces the offset to move in the positive direction and that FN stressing under low -VO2 condition forces the offset to move in the negative direction.

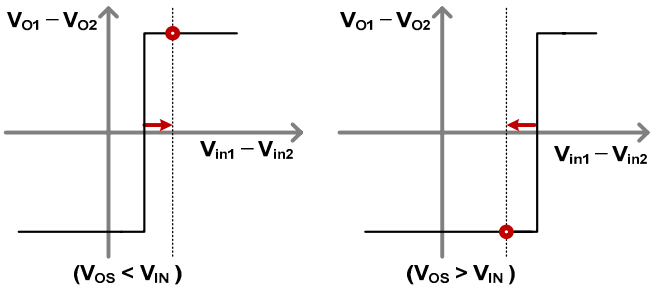

Fig. 6 Offsets can be driven to a wanted value by applying non-zero input voltage.

Many comparators have a pre-amplifier stage especially in high performance analog circuits in order to prevent the kick-back noise. To apply our method of the offset manipulation efficiently to the comparator with a pre-amplifier stage, the gain of the pre-amplifier should be low, not much higher than unit. This offset manipulation can only be applied to the latch stage. Offset of the latch stage is divided by the gain of pre-amplifier when referred to the comparator input. Therefore, the whole comparator offset can hardly be manipulated if the pre-amplifier gain is high.

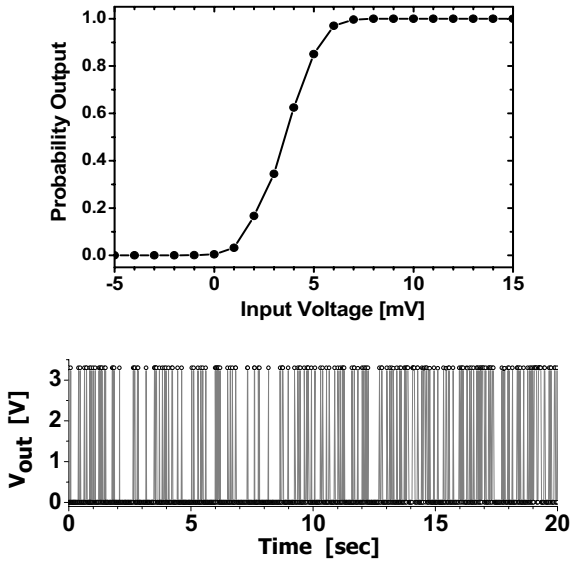

Fig. 7 Probability transfer curve of a latch-type comparator with an about 4mv offset and a measurement example at 0.2

5. Test Results

Offset value of a comparator can be measured from the input – output transfer curves. However, in real situation exists random noise which makes it impossible to define an abrupt trip-point. Instead, we can obtain the output-1 ratio depending on the input voltage. Thus, the comparator transfer can be described by probability transfer curve. Fig. 7 shows a measured probability transfer curve. At a certain input voltage, the comparator produces output-1 or 0 voltages at a specific ratio. The offset value is estimated as the input voltage where the probability output is just 0.5. And the range of transition region indicates the magnitude of the random noise in the comparator.

Fig. 8 shows the stress-packet process that a comparator offset is being eliminated. In the beginning, only the zero outputs have been observed. As the stress-packet task proceeds, the 1 output begins to show up and becomes more frequent, which means that the offset approaches to the same value as the input voltage.

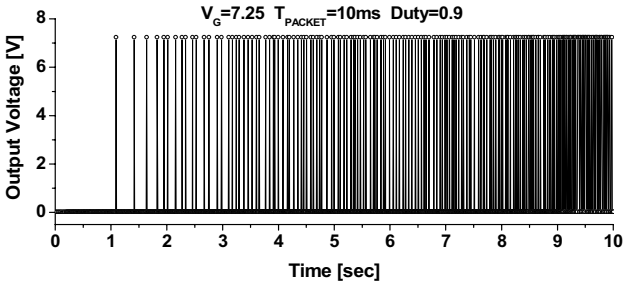

Fig. 8 As the stress-packets are performed on the test comparator, the probability outputs approaches to 0.5.

6. ROM Applications

Advantage of zero offset is clear. It enhances performance of precise analog circuits and reduces the probability of erroneous operations at memory circuits.

Intentional offset implantation by the stress-packet method also can be very useful. A comparator produces the output voltage at zero input according to the offset's sign as shown in Fig. 2. This can be utilized as a non-volatile memory cell. One can program this memory cell by stress-packet operation under a positive or a negative input voltage.

For the memory cell application, the comparator must be simple above all. Therefore, the latch-type comparator treated in this paper is best fit for it. As the offset is the physical quantity that stores binary data in this offset memory, it shows non-volatile data retention.

Recently, one-time programmable (OTP) memories are attracting people's attentions, where firmware programs of the system-on-chips (SoC) are programmed and stored. This kind of memory should be implemented in the standard CMOS process so as to minimize the fabrication costs. So far, the OTP memories belong to the category of the anti-fuse, using the thin oxide destruction phenomena.[8-10] Consequently, the programming is allowed by only one time.

Our offset memory can be implemented in the standard CMOS process. The biggest advantage of our offset memory over the conventional OTP is that programming is possible by multiple times. As shown in Fig. 1, the threshold voltage of MOS transistors can shift by hundreds of mili-volts. For

cell programming, only 20~30mV of comparator offset is expected to be sufficient because the offset have only to have the margin against the offset drift and the random noise. Therefore, it is possible to re-program the programmed cell by shifting the offset from 30mV to -30mV, for example. This property may be very useful for SoC's in that the firmware can be updated in the field. Of course, the number of re-programming is restricted. According to our experiments, though the possible number of re-programming is varied from process to process, programming is repeatedly performed on a cell at least 3~5 times.

Other advantages of the offset ROM are the low voltage operation and the simple read circuit. The latch comparator is a digital circuit so that it stably works even below 0.5V supply voltage. And the latch is a regenerative circuit so that the offset ROM circuit will not need sense amplifier circuits.

Fig. 9 shows one possible cell array circuit of the offset ROM memory and its timing plot for programming operation. The latch enable signals, LEN and LEP, run in the column and row directions, respectively, which prevent stressing the non-selected cells. The LEN signal is on the V_{CC} level when it is not selected. Therefore, the stress-voltage is lower by V_{CC} for the cells of non-selected columns, where the programming disturb is neglible.

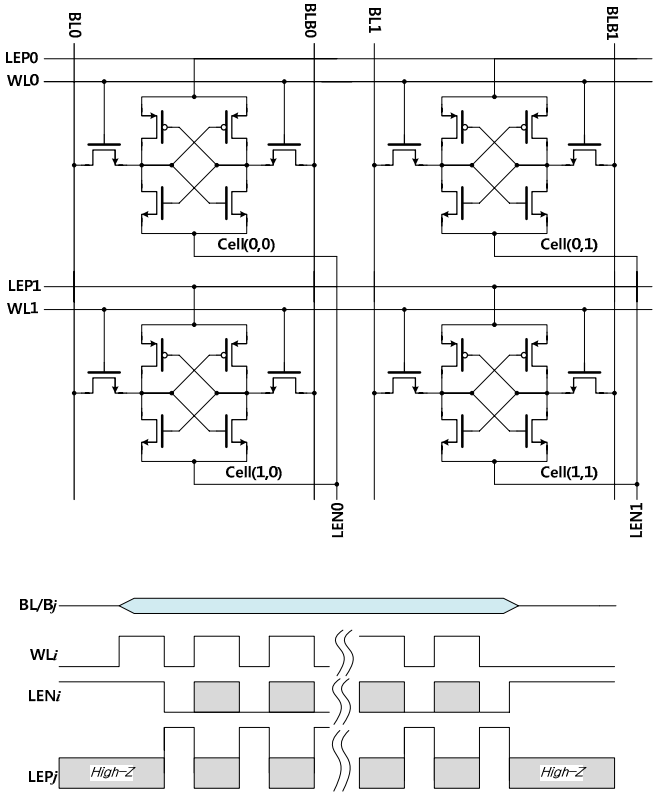

Fig. 9 One possible cell array circuit of the offset ROM memory and its signal timing plots for programming operation.

7. Conclusions

In this paper, we have suggested a method to intentionally manipulate offsets of comparator circuits. It makes use of the well-known FN stress degradation phenomena of the MOS transistors for altering threshold voltages, thus, the offset voltage. This method does not increase circuit area nor degrade timings. The comparator offset is adjusted to the same value as the applied input voltage through the stress-packet method. We can utilize it for a non-volatile memory cell as well as for cancelling comparator offsets.

This method can show versatility in various application fields. However, further researches on device reliability are necessary for the stable employment in industrial fields, including oxide breakdown, offset drifts, scaling properties, etc.

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