Logarithmic and Antilogarithmic Circuit with Gate – to – Substrate Biasing Technique

Sanchai Harnsoongnoen[1], Chiranut Sa-ngiamsak[2], Poonsak intarakul[3] and Rardchawadee Silapunt[4]
[1]Department of Electrical Engineering, Khon Kaen University, Khon Kaen, 40002, Thailand
[2]Department of Electrical Engineering, Khon Kaen University, Khon Kaen, 40002, Thailand
[3]Department of Radiology, Khon Kaen University, Khon Kaen, 40002, Thailand
[4]Department of Electronics and Telecommunication Engineering, King Mongkut's University of Technology Thonburi, Bangkok, 10140, Thailand
E-mail: [1]4750400079@kku.ac.th, [2]chiranut@kku.ac.th, [3]poonsak.medphy@gmail.com, [4]rardchawadee.sil@kmutt.ac.th

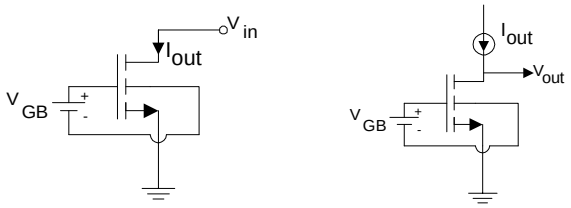
Abstract: This is a report on a high frequency response and low static power dissipation logarithmic and antilogarithmic circuit generated by a single MOS transistor operating in a weak inversion mode with the gate–to–substrate (G-B) biasing technique. A comparison of the simulation results and the measurements is shown in this paper. The simulation results are generated by PSPICE with AMS 0.8µm technology. The simulation results are also compared with the case of conventional biasing technique. The comparison intriguingly reveals that the frequency response of the proposed circuit is 45k times higher than that of the conventional circuit; its static power consumption is zero watt due to none of biasing current to operate the device when there is no input signal.

1. Introduction

Logarithmic and antilogarithmic functions are widely used in many applications; for example, instrumentations, telecommunications, neural networks, medical equipments, active filters, and arithmetical operation circuits etc [1-9]. Traditionally, logarithmic and antilogarithmic function circuit are genearted by using Operation Amplifier (Op-Amp) [1-3], bipolar transistor [4,5] and MOS transistor operating in a strong inversion mode [6]. The draw backs of the above technique are high power consumption, expensive, complexity and large silicon area. Power consumption concern of log and anti-log functions with MOS technology is eased when MOS operation is in weak inversion. Nevertheless, its consequence is the limitations to low speed and low frequency applications. To enhance a frequency aspect, MOS operation in strong inversion with a pseudo-exponential and translinear circuit was introduced, but the pay-off is the higher number of MOS devices and hence power consumption. This work proposes a high frequency and low static power dissipation logarithmic and antilogarithmic circuit by using the G-B biasing technique on a single MOS transistor operating in weak inversion.

2. G-B biasing technique Principle

The design of a logarithmic and anti-logarithmic circuit using Gate-to-Substrate, G-B (where the subscript B denote the bulk silicon) biasing technique has been introduced by Al-Absi [10]. In this technique, Gate-to-Substrate is used for biasing transistor; and the input signal is applied at the drain terminal either as voltage or current as shown in Fig.1.



(a) (b)

Fig.1 G-B biasing technique
(a) antilogarithmic circuit (b) logarithmic circuit

3. Experimental method

Logarithmic and antilogarithmic functions ofthe proposed circuits were confirmed by measurements. The I-V characteristics of an n-channel MOS transistor verified the validation of the proposed idea. Specimen were fabricated using a standard 0.8µm CMOS process with polysilicon gates with gate oxide thickness t_{ox} of 25 nm; and shallow trench isolation was used. A constant gate width, W = 40µm and gate lengths, L = 0.8 µm. The DC characteristics were measured using the HP4156B precisions semiconductor parameter analyzer. I-V characteristics measurements were performed on wafer in a shielded probe station. Experimental setup is shown in Fig.2.

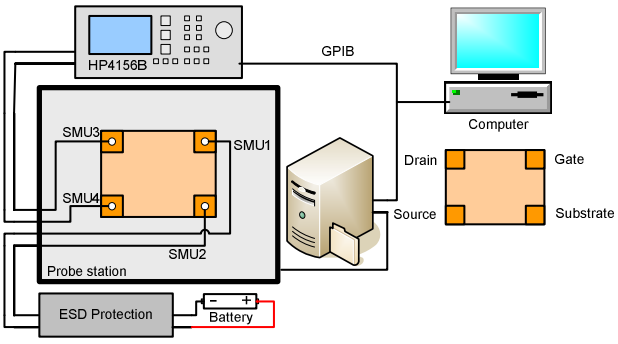
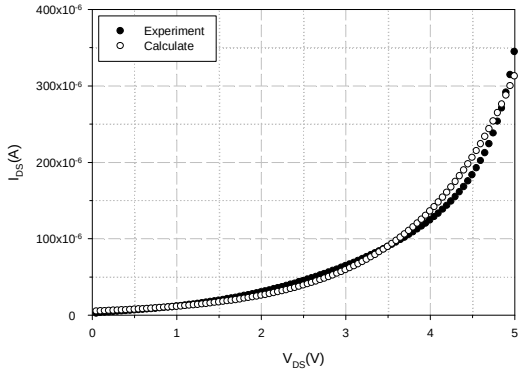


Fig. 2 Configuration of measurement

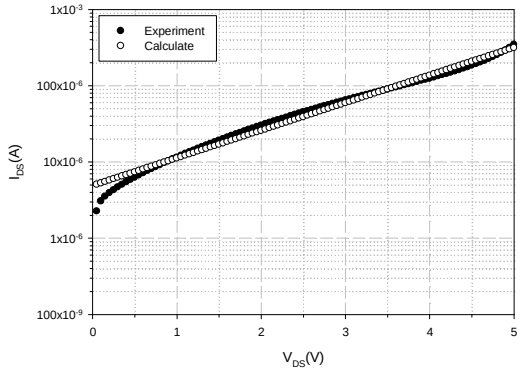
4. Experimental Results

An n-channel MOSFET was biased with our proposed configuration of $V_{GB} = 0.7V$ to ensure its mode of operation is in weak inversion mode. An anti-logarithmic

function is achieved when input signal is voltage signal, V_{DS} while a logarithmic function is attained when input signal is current signal, I_{DS}. Fig. 3 and Fig.4 depict the I-V characteristic of the MOS operating under our proposed configuration for anti-log and log functions, respectively. A solid line represents measurement while a dot-line represent a simulation result based on theory of MOS operating in weak inversion.

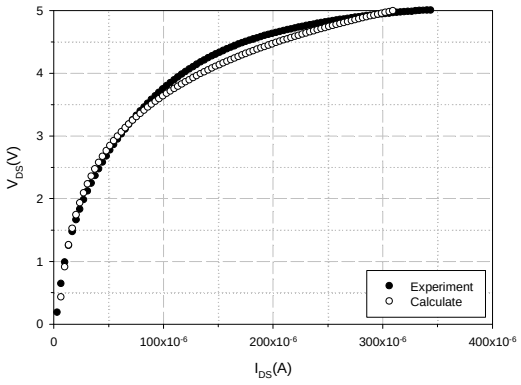


(a) Linear scale

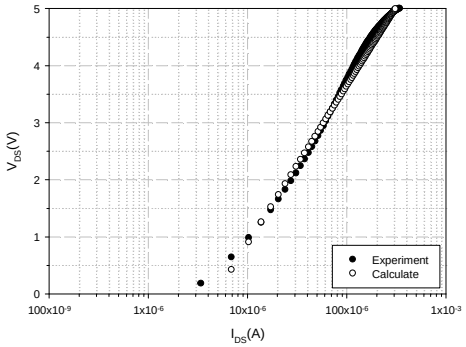


(b) Log scale

Fig. 3 Input signal applied is voltage (V_{DS})



(a) Linear scale



(b) Log scale

Fig. 4 Input signal applied is current (I_{DS})

The well-known drain-source current of MOS in weak inversion is given below [11]:

$$I_{DS} = I_{DO} \cdot e^{\frac{V_G - n \cdot V_{DS}}{n \cdot V_t}} \quad (1)$$

where

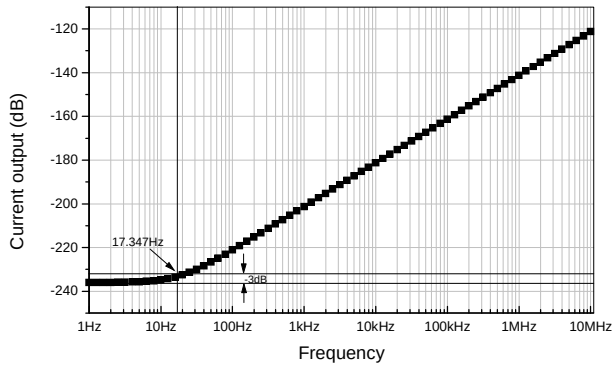
V_G is Gate-Body voltage,
V_T is the thermal voltage = $k \bullet T / q$
I_{DO} is the specific current = $2 \bullet n \bullet \beta \bullet V_t^2$
β is the transfer parameter = $\mu \bullet C_{ox} \bullet W_{eff} / L_{eff}$
and n is slop factor of curve

Eq(1) shows that the I_{DS} is an exponential function with the V_{DS}; and logarithemic function occurs when the input signal is the V_{DS}. The comparison between the measurements and simulation based on theory do agreee with each other.

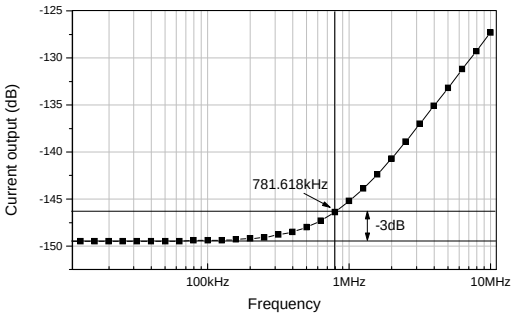
The major contribution of this work is its high frequency response of log and anti-log functions genearted by MOS with weak inversion. The figure of merit of frequency response is verified by simulation results run on PSPICE. A set of SPICE parameters for simulator was chosen from AMS 0.8µm CMOS technology. The comparison of the frequency response between the proposed configuration and the conventional technique with weak inversion is depicted in Fig.5. AC voltage of 1Vp-p was applied to the simulator; and the operating frequency was swept upto 10MHz. The output signal, I_{DS} for an anti-log configuration and V_{DS} for a log configuration were monitored. Fig. 5(a) shows the cut-off frequency of a conventional technique (17.347Hz) and Fig. 5(b) and 5(c) are shown the cut-off frequency of the proposed configuration of the antilogarithmic (781.618kHz) and the logarithmic circuit (784.750kHz) respectively. The results in Fig.5 clearly exhibit the superior frequency of the proposed configuration comparing with that of a conventional. The cut-off frequency of this work is almost 45k times better than a conventional.

Another way to exhibit a long and anti-log functions of the proposed configuration operating in high frequency, the plot of a voltage input and a current output is shown in Fig.6. The input signal voltage is a 200mV peak to peak

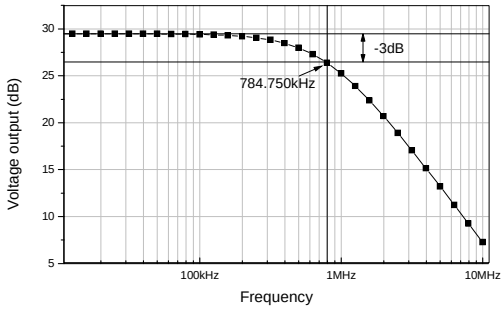
triangular wave of 780 kHz frequency. The corresponding output is still parabolic. Moreover, additional advantage of the G-B biasing technique is that the static power dissipation is zero since the there is no current drawn from the bias voltage.



(a)

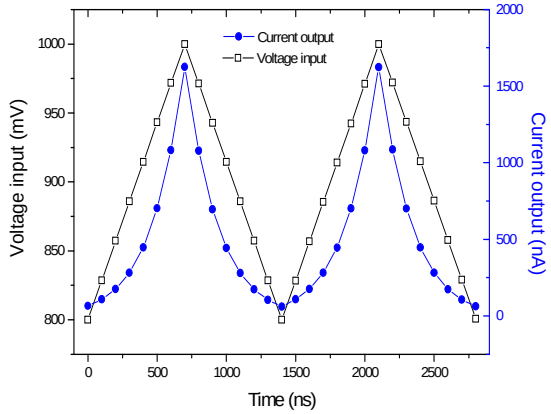


(b)

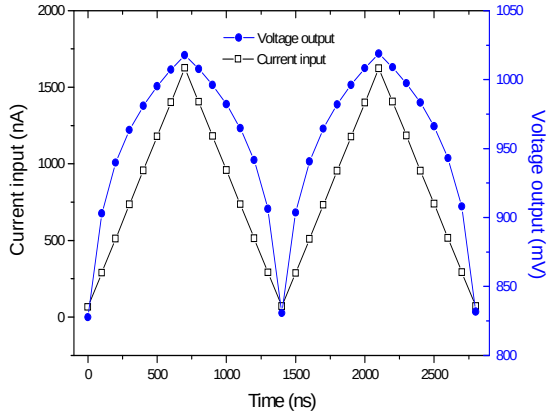


(c)

Fig. 5 frequency response of the MOS transistor (a) conventional biasing (b) G-B biasing technique (antilogarithmic) (c) G-B biasing technique (logarithmic)



(a)



(b)

Fig. 6 simulation results for "antilogarithmic (a) and logarithmic (b)" a triangular input wave form

5. Conclusions

High frequency response and low static power dissipation of a logarithmic and antilogarithmic circuit using G-B biasing technique in weak inversion have been investigated. The simulation and measurement results reveal that, a relationship between I_{DS} and V_{DS} is in logarithemic form due to the mode of operation is in weak inversion. The simulations, calculations and measuremetns agree with each other. Moreover, this technique offers a high speed frequency of operation and zero static power dissipation with the gate-to-substarte biasing technique. .

References

[1] A.B. Grebene, "Bipolar and MOS integrated Circuit Design", John Wiley & Sons, New York.1984.

[2] D.L. Grundy, "A computational approach to VLSI analog Design", journal of VLSI signal processing, 8, pp.53-60,1994.

[3] Y.B. Acharya and P.D.Vyavahare, "A low-current logarithmic LED electrometer", IEEE Trans. Inatrum. Meas.,49, pp. 5-9, 2000.

[4] R.F. Wolffenbuttel,"Digitally programmable accurate current source for logarithmic control of the amplification

or attenuation in again cell", IEEE J. Solid-State. Circ., Vol.23, pp.767-773,1988.
[5] K. Kumwachara, "Low voltage current mode power factor function generator", IEICE Trans. fundamentals, Vol. E83-A, No.2, pp.172-177, 2000.
[6] A. Motamed, C.Hwang and M.Ismail, "CMOS exponential current-to-voltage converter," electronics letter, Vol.33 No.12, pp.998-1000, 5th June, 1997.
[7] C. Mead, "Analog VLSI and neural systems", Addison-Wesley, 1989.
[8] L. Moini, "Vision chips or seeing silicon", third revision, chapter 7, 1997.
[9] F. Bergouignan, N. Abouchi, R. Grisel, G. Caille and J. Caranana, "Designs of a logarithmic and exponential amplifiers using current conveyors", the third IEEE international conference on electronics circuits and systems(ICECS'96), Rodos, Greece, pp.61-64, 1996.
[10] M. Al-Absi, "A new biasing technique for the MOS transistor and its applications in analogue IC design". PhD Thesis, UMIST, Manchester, 2002.
[11] G.A.S. Machado, C.C Enz and M. Bucher, "Estimating key parameters in the EKV MOST model for anlalogue design and simulation", proc. Of the IEEE Int. Symposium on circuits and systems, pp.1588-1591, 1995.