A 1㎒ High Efficient, Two-Stage Interleaved Synchronous Buck CMOS DC-DC Converter

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Abstract: This paper presents a high efficient 3.3 – 1V two-stage interleaved synchronous buck CMOS DC-DC converter designed with standard CMOS 0.35μm process parameter. The proposed circuit has a low output voltage ripple. To reduce the output voltage ripple, the duty cycle of the interleaved converter is fixed as D=0.5 by an input stage buck converter. It causes the best ripple cancelation of the output current ripple. The proposed circuit was simulated by HSPICE and the simulation results show that the efficiency of the proposed converter is more than 85% in the load current range of 125 – 400mA, and the peak-to-peak output voltage ripple is measured as 10 mV with the 1μF external output capacitor. From these results, the proposed circuit is adequate for the battery-operated system.

1. Introduction

Mobile devices, such as digital camera, cellular phone, MP3 player, and PMP (portable Multimedia Player) are in great demand in today's consumer market. And these devices demand smaller and lighter weight power supplies and extended battery lifetime. In small form factor mobile devices, efficient power regulation and distribution to each component on the chip is a critical issue [1].

In the switched-mode converter, there is an output voltage ripple by switching. It becomes a critical issue because the supply voltage is getting lower. There are lots of methods to reduce the output voltage ripple. But, SM power supply makes a current ripple because of the operation properties, which should make the output voltage ripple. The interleaved DC-DC converter, that operating with opposite phase to parallel inductors, can reduce the output current ripple sufficiently. Using the interleaved method, the power losses of the magnetic core and power switches can be reduced significantly; furthermore, it can use smaller size magnetic cores and power switches. Another remarkable advantage is the synthesized switching frequency of the output stage that can be higher than the switching frequency of a single DC-DC converter. Therefore, the ripple current at the output capacitor can be reduced to meet the ripple voltage requirement. But, the output current ripple is much bigger when the duty cycle is more different from 0.5.

In this paper, a high efficient two-stage interleaved synchronous buck DC-DC converter with the fixed duty cycle is presented. The DC-DC converter is designed in standard CMOS 0.35μm process parameter. The proposed converter achieves 88.7%, at the output current of 250mA. Section 2 describes the proposed converter's configuration and operation principles. The HSPICE simulation results to veryfy perfomance of the converter are presented in section 3. Conclusions and future work are discussed in section 4.

2. Circuit Principle and Operation

2.1 Two-stage Interleaved Buck Converter

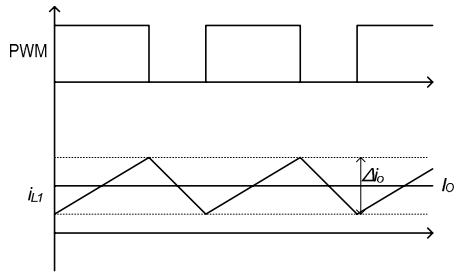

Figure 1. Waveforms of synchronous buck converter

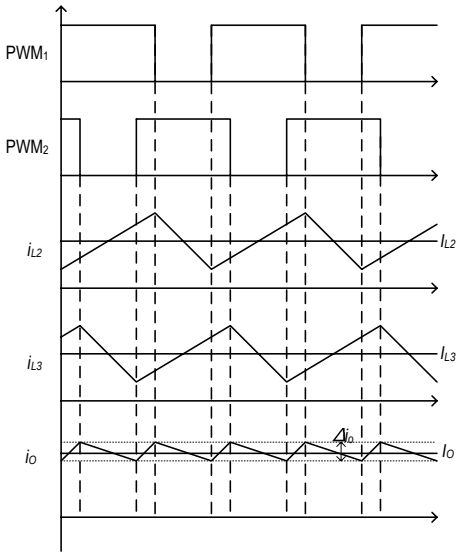

Figure 2. Waveforms of the two-stage interleaved synchronous buck converter

Figure 1 shows an inductor current of a buck converter using PWM method. It has a current ripple, Δi_o, and it causes a voltage ripple at the output. The interleaved converter is proposed to reduce this current ripple. Figure 2 shows an inductor current waveform of the interleaved buck converter. The key principle of the interleaved buck converter is to cancel out the freewheeling current and the turn-on current. That is, the turn-on current flows through

one channel, and freewheeling current flows through the other channel at the same time. The amount of the inductor current ripple is given by equation (1), where N, L_f and T_S are the channel number, the output inductance per channel and the switching period, respectively. M = floor(N · D) is the maximum integer that does not exceed the N · D [3].

$$\Delta i_o = \frac{V_{out}(1-D)T_S}{2L_f}\frac{N\left(D-\frac{M}{N}\right)\left(\frac{M+1}{N}-D\right)}{D(1-D)} \quad (1)$$

From equation (1), we can find out the output current ripple cancelation depends on N and D. The first term in equation (1) is the inductor current ripple, and the second term represents the effect of N and D on the current ripple cancelation.

$$\Delta i_{on} = \frac{\Delta i_o}{\frac{V_{out}T_S}{2L_f}} = \frac{N\left(D-\frac{M}{N}\right)\left(\frac{M+1}{N}-D\right)}{D} \quad (2)$$

Equation (2) gives the output current ripple, Δ i_{on}, which is normalized to the inductor current ripple at D=0 as a function of D and N.

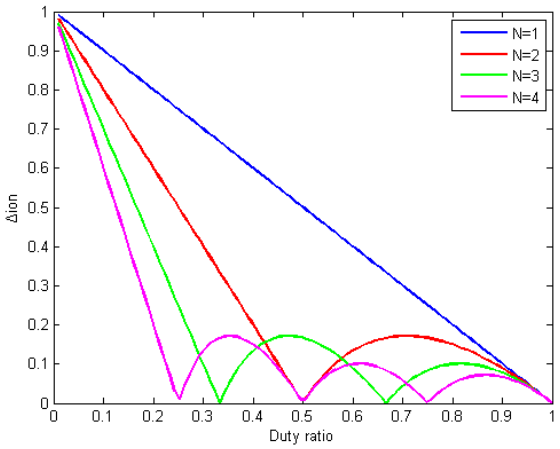

Figure 3. Output current ripple cancelation as a function of D

Figure 3 shows Δ i_{on} for different values of N. For a two-stage interleaved converter, the ripple is totally canceled out when D=0.5. With small duty cycles, the current ripple reduction is poor. Assuming that all of the ripple components of the output current flows through the filter capacitor C_f and its average components flows through the load resistor, the peak-to-peak output voltage ripple, Δ V_o, can be written as equation (3) [1].

$$\Delta V_o = \frac{1}{C_f}\frac{1}{2}\frac{\Delta i_o T_S}{2N} = \frac{V_{out}(1-D)T_S^2}{8C_f L_f}\frac{\left(D-\frac{M}{N}\right)\left(\frac{M+1}{N}-D\right)}{D(1-D)} \quad (3)$$

The output voltage of a buck converter depends on D and V_{in} as equation (4). The output voltage of a buck converter is varied by the variation of the input voltage and the output current. It makes the duty cycle changed and this causes a poor current ripple cancelation of the interleaved converter.

$$V_{out} = D \cdot V_{in} \quad (4)$$

In this paper, to achieve the best output current ripple cancelation, the duty cycle is fixed as 0.5 by an input stage buck converter. Figure 4 represents the proposed circuit.

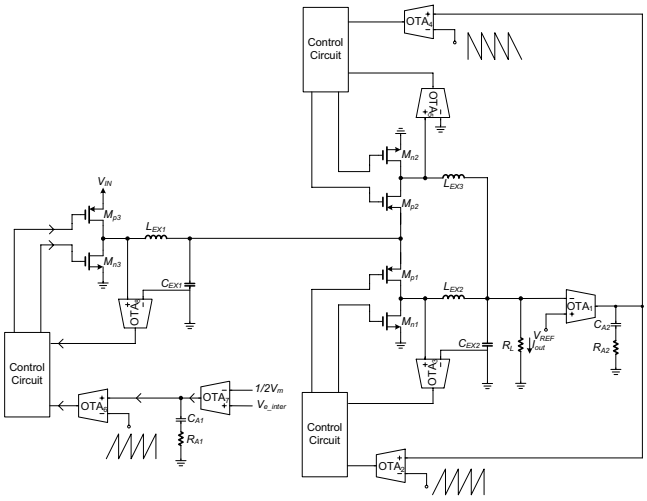

Figure 4. Circuit diagram of proposed circuit

The proposed interleaved buck converter consists of an error amplifier, switching control circuits, comparators for the zero current detection, PWM signal generators, and the input stage buck converter.

2.2 PWM signal generator

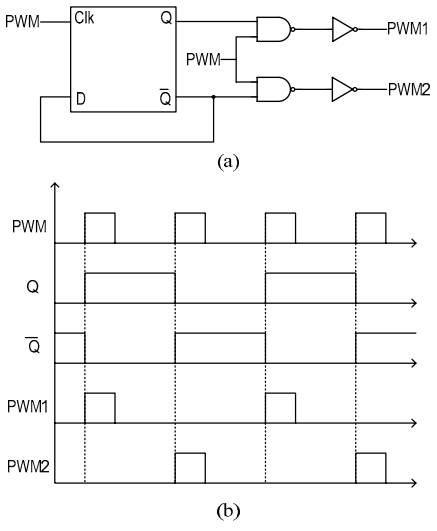

Figure 5. Conventional PWM signal genarator (a) circuit diagram (b) timing diagram

PWM signals of each channel have phase delay between them in the interleaved buck converter. And it make an output current ripple cancelation as mentioned before. Figure 5 shows a circuit diagram and timing diagram of the PWM signal generator in [1]. In this circuit, the duty cycle

of the original PWM signal must be almost 1 to achieve a 0.5 duty cycle at the each channel with a two-stage interleaved converter. This circuit is more efficient in that has more channels. For individual two PWM signals, we use two kinds of saw-tooth waves, one has a positive slope and the other has a negative slope in this paper. Figure 6 represents the timing diagram of two saw-tooth waves. Those waves make the same duty cycle PWM signals which have a phase delay between them.

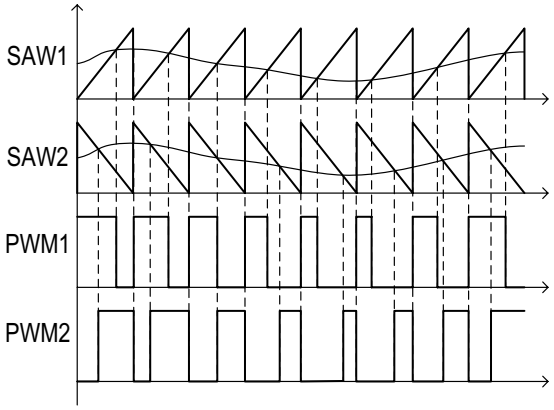

Figure 6. Timing diagram of PWM generator

2.3 Switching control circuit

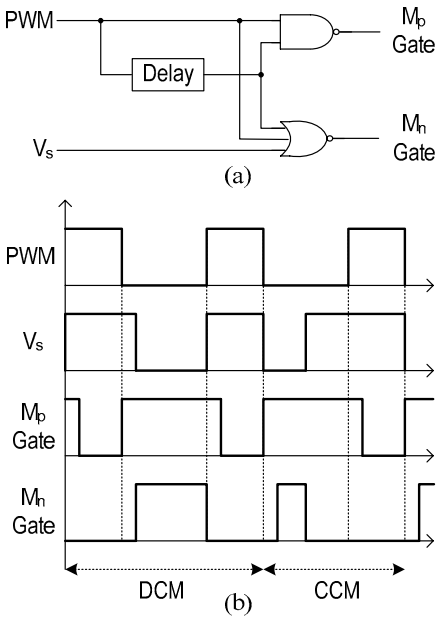

Figure 7. Swtching control (a) circuit diagram and (b) timing diagram

Since n-channel MOSFET is used in the output stage instead of a shottkey diode, it is able to turn on both power MOSFET. And it will cause lots of power dissipation and unstable operation of all circuitry blocks. To avoid this, the switches have to be controlled by non-overlapping signals. Figure 7 shows the circuit diagram of the switching control circuit and its timing diagram in the continuous current mode (CCM) and the discontinuous current mode (DCM). Another problem is the reverse current flow, which is occurred under the light load condition. When the load is light, the converter operates in DCM. In the DCM, the energy stored in external inductor is small. This energy is released to the load when the n-channel MOSFET is turned on. So without the reverse current protection circuit, reverse current flows through the n-channel MOSFET discharging stored energy in the external capacitor. To avoid this, switching circuit turns off the n-channel MOSFET when the inductor current reaches zero. It is detected by a comparator. In the figure 7, V_S means the output of the zero current detecting comparator.

2.4 Input stage buck converter

As mentioned before, it has the best output current ripple cancelation at D=0.5 in the two-stage interleaved buck converter. To achieve the fixed duty cycle as D=0.5, we put the buck converter which follows the duty cycle of interleaved buck converter, the duty cycle of the buck converter is controlled by that of the interleaved buck converter. Figure 8 shows the input stage buck converter.

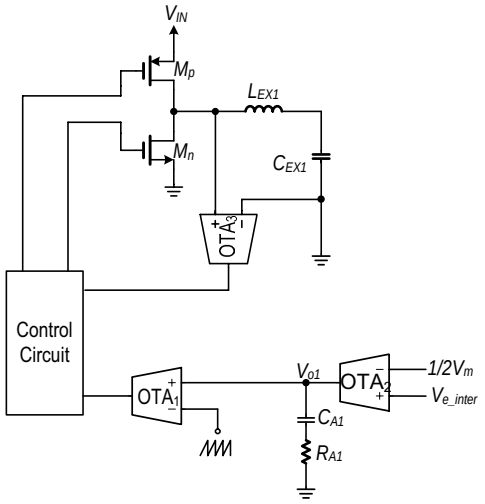

Figure 8. Circuit diagram of the input stage buck converter

The input stage converter consists of two MOSFET switches M_p and M_n, an external inductor L_{EX1}, an external capacitor C_{EX1}, OTA error amplifier, OTA comparators, and a switching control circuit. OTA_1 compares the output voltage of the error amplifier, V_{o1}, with saw-tooth wave and generates the PWM signal. Then the duty cycle, D, of the PWM signal is given by equation (5).

$$D = \frac{V_{o1}}{V_M} \qquad (5)$$

From equation (5), the duty cycle of PWM signal follows the output of the error amplifier. If the output of the error amplifier is same as a half of the saw-tooth wave peak-to-peak amplitude, V_M, then the duty cycle is 0.5. We use this relation to achieve a fixed duty cycle. The error amplifier compares the error of the interleaved converter with a half of the V_M. When the error is lower than $1/2V_M$, the output

voltage of the error amplifier, V_{e_inter}, is decreased and the output voltage of the input stage converter is decreased. Thus the duty cycle of the interleaved converter is increased. And the other case, error is higher than $1/2V_M$, the output voltage of the input stage converter is increased and the duty cycle of the interleaved converter is decreased. In both case, the output voltage of the interleaved converter is regulated by its feedback control. Thus, the output voltage regulation of the interleaved converter with fixed duty cycle is realized.

3. Simulation Results

HSPICE simulation program was used to verify the operation of the proposed circuit with standard CMOS 0.35μm process parameters. The supply voltage, V_{in}, was 3.3V, reference voltage, V_{ref}, was 1V and peak-to-peak voltage of saw-tooth wave, V_M, was 2V. The external inductor and capacitor of the input stage buck converter were 8μH and 2μF. The external inductor and capacitor of the interleaved converter were 10μH and 1μF for each channel. Figure 9 shows PWM signals and the output current and the inductor currents of each channel. The peak-to-peak output current ripple was measured as 2.5mA at 250mA output current. Figure 10 shows the simulated efficiency of the proposed converter versus its load current. More than 85% efficiency is shown in the range of 125 – 400mA.

4. Conclusion

This paper presents the two-stage interleaved synchronous buck DC-DC converter with the fixed duty cycle by the added buck converter for the low output voltage ripple. Its operation and performance were verified by HSPICE simulation. The peak-to-peak output voltage ripple is measured as 10mV. More than 85% efficiency of the converter was shown so that the converter is adequate for a battery operation system. The fabrication of the proposed converter using 0.35μm CMOS process and replace the added buck converter with an inductorless converter should be the subject of future studies.

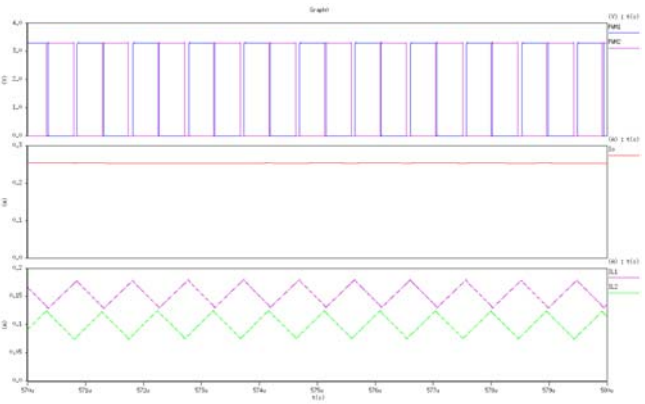

Figure 9. Simulated waveforms at various nodes

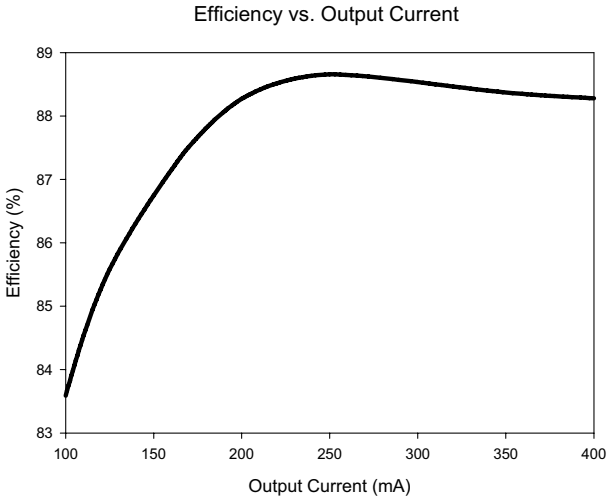

Figure 10. Efficiency vs. Ouput Current

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