A High Efficiency Boost Converter For TFT-LCD Bias Supply

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***Abstract*—In this paper, a high efficiency boost converter is designed using a 0.5-μm 5V, 3.5-μm 30-V CMOS process for TFT-LCD Bias supply. The boost converter can be adjusted with external resistors. The boost converter's input power supply range is 2.5V $\sim$ 5V, the output voltage range is 10V-20V and the clock frequency is 1.3 MHz. The maximum load current is 120mA at an input power supply of 3V, output voltage of 20V and the maximum efficiency is 92% with input power supply at 5V, output voltage of 12V, and load current of 120mA. The simulation results show the successful operation of the boost converter.**

I. Introduction

WITH the increasing popularity of portable devices, customers continue to demand longer battery runtime, smaller size, and lower cost. Based on these demands from the marketplace, optimized DC-DC converters are essential in order to supply power efficiently to support various mobile device functions [1]. Especially the demand for power management circuits for LCD displays, for notebooks, personal digital assistants, and pocket PCs, is increasing. Accordingly, in this paper, the optimized boost converter for TFT LCD bias is designed with current mode control.

A charge pump or a switching regulator circuit is generally used to generate a voltage higher than the supply voltage. Whereas a charge pump circuit uses a capacitor to store energy, a switching regulator uses an inductor. The latest mobile devices require high power consumption, which calls for a switching regulator type boost converter with a high efficiency even at significant load currents.

Both voltage mode and current mode controls are commonly used to design DC-DC converters. With a narrower bandwidth than the current mode control, voltage mode cannot quickly respond to abrupt changes in output voltage and current. Furthermore, two poles, generated by the external inductor and capacitor used as the low pass filter, complicate the compensation circuit structure, making it difficult to secure stability of the overall circuit. On the other hand, current mode control has wider bandwidth than voltage mode, enabling quick response to abrupt changes in output voltage and current. The second pole is also nearer to the switching frequency, which simplifies the compensation circuit. However, in addition to the loop for detecting the output voltage, current mode control requires another loop circuit for detecting the inductor current. Furthermore, if the duty cycle is greater than 0.5, the entire circuit becomes unstable. Therefore, an artificial ramp signal is required to solve the stability problem [2]- [3]. In this paper, the boost converter is designed with current mode control to provide wide bandwidth and, good line and load regulation.

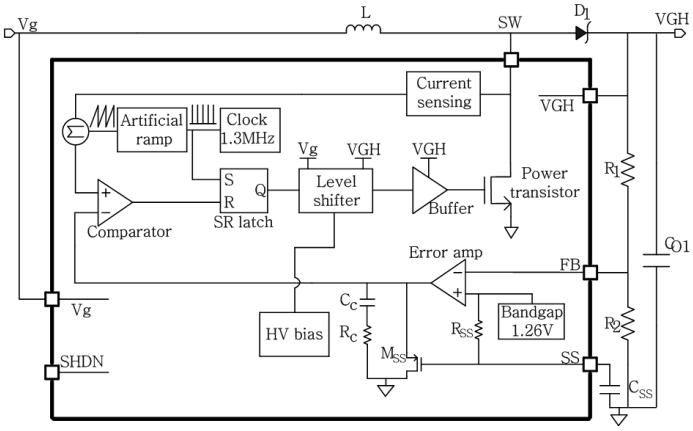

Fig. 1. Block diagram of the designed boost converter.

II. Boost converter circuit

Fig. 1 shows the designed boost converter. The region surrounded by dark lines is the on-chip integrated controller of the boost converter. The boost converter control circuit contains a soft-start circuit that consists of bandgap, R_{SS}, M_{SS} and C_{SS} to prevent any inrush current [4]. The compensation circuit for achieving overall boost converter loop stability consists of the error amplifier, C_C and R_C. The artificial ramp circuit prevents instability when the duty cycle exceeds 0.5, and the clock generator provides the clock signal required for the entire system. The SR latch generates the pulse-width modulation (PWM) signal, and the level shifter and the buffer circuit are implemented to deliver the PWM signal to the power transistor. There is also an inductor current sensing circuit, and the high-voltage (HV) bias circuit to supply bias current to the high-voltage blocks.

To briefly explain the overall mechanism of the boost converter, when there is an abrupt transition from a light load to a heavy load, the boost converter's output voltage drops and the feedback (FB) node voltage also decreases according to the resistance ratio. The decreased feedback voltage raises the error amplifier output voltage, which the comparator compares

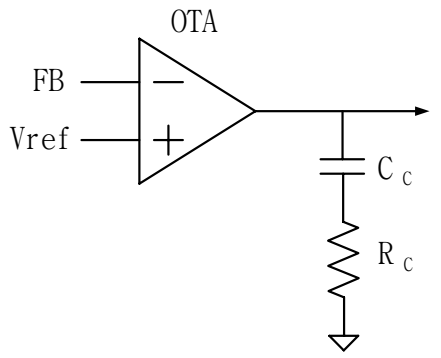

Fig. 2. Compensation circuit.

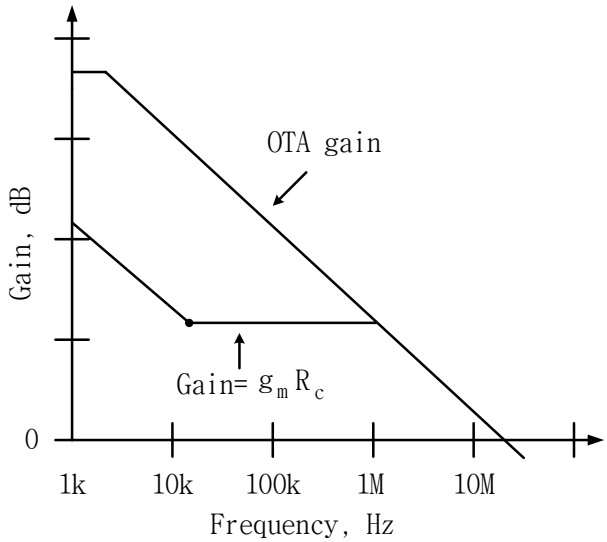

Fig. 3. Frequency characteristic of the compensation circuit.

with the sum of the current sensing and artificial ramp signals. The error amplifier's increased output signal slows down the reset time of the SR latch, which controls the PWM duty cycle. The generated PWM signal then increases the inductor current through the level shifter and buffer circuits and compensates for the output voltage decreased by the heavy load. If there is a transition from a heavy load to a light load, the circuit operates in the opposite manner.

A. Compensation circuit

The compensation circuit and its frequency characteristic are shown in Fig. 2 and 3, respectively. The designed boost converter circuit is controlled in current mode, and the second pole is closer to the switching frequency making compensation simpler than for a voltage mode converter. A simple proportional integral (PI) compensation circuit is used [6], and overall stability of the boost converter can be achieved by positioning the reference point at a desired spot using R_C and C_C values. The equation for compensation circuits can be expressed as follows:

$$A_v = G_m \times R_{out}(1 + \frac{s}{\omega_z}) \tag{1}$$

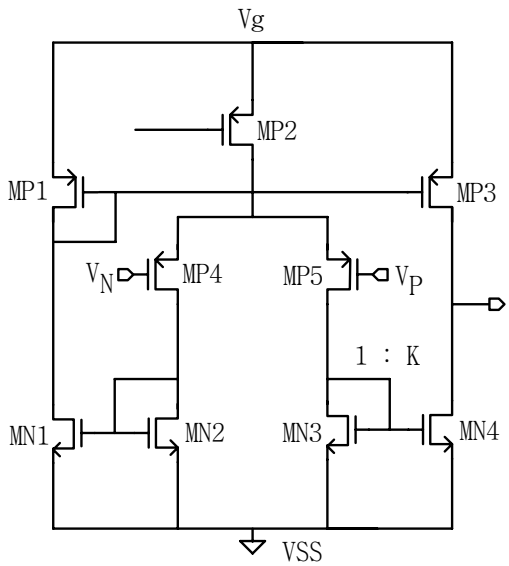

Fig. 4. Operational transconductance amplifier (OTA).

$$\omega_z = -\frac{1}{R_c \times C_c} \tag{2}$$

where G_m and R_{out} denote the transconductance and output resistance of OTA, respectively.

The converter's unity gain frequency set by the feedback loop is usually set within 20 % of the switching frequency to reduce the effect of switching noise. For the purposes of this paper, adequate R_c and C_c values were selected to achieve a phase margin of 60 degrees at Vg=3V, VGH=10V and load current=100mA. Fig. 4 shows the OTA structure used in the compensation circuit. The OTA transconductance G_m can be written as follows [7]:

$$G_m = \frac{I_{out}}{V_P - V_N} = K \times g_{mp4,5}. \tag{3}$$

B. Clock and Ramp Generator

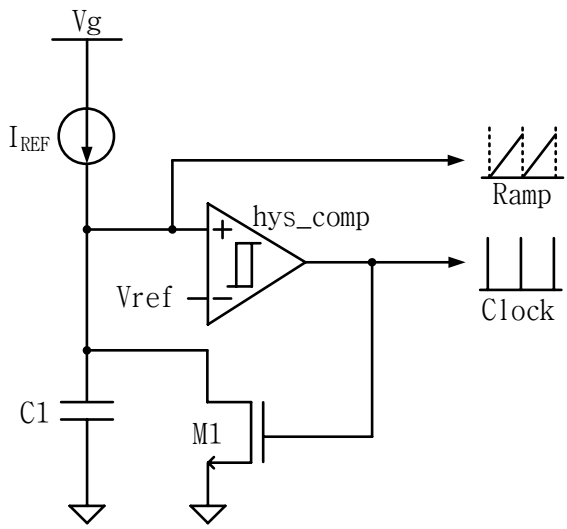

Fig. 5. Clock and ramp generator.

TABLE I
PERFORMANCE SUMMARY OF THE SIMULATED BOOST CONVERTER.

Process	0.5-μm 5V, 3.5-μm 30V
Switching frequency	1.3MHz
Supply voltage	2.5V $\sim$ 5V
Output voltage	10V $\sim$ 20V
Efficiency(MAX)	92% @ Vg=5V, VGH=12V, Iout=120mA
Core area	2150μm $\times$ 2150μm

Subharmonic oscillation is a well-known problem for current mode switching converters with the duty ratio D larger than 0.5. To avoid subharmonic oscillation, the slope of the compensation ramp m_a must be larger than half of the slope of inductor current m_2 during the second subinterval $\bar{D}T$. The value of m_a is generally determined as follows [8]:

$$m_a \geq \frac{m_2}{2} \tag{4}$$

where m_2 denotes the slope $(Vg - VGH)/L$ in the region where inductor current decreases.

The circuit for generating the artificial ramp signal and the clock signal is shown in Fig. 5. The slope of the artificial ramp is determined by I_{REF} and C1. When I_{REF} from the current source charges the capacitor C1, the voltage at the ramp node increases at a fixed rate $I_{REF}/C1$, which is equal to the slope m_a. If the increasing ramp signal reaches V_{ref}, the output node of the hysteresis comparator switches from low to high and the clock also becomes high. Once the clock switches to the high state, it turns on transistor M1. In turn, C1 is discharged and the ramp node voltage decreases. When the ramp node voltage decreases to the low boundary of the hysteresis comparator, its output switches from high to low, the clock drops to the low state, and M1 is switched off, triggering I_{REF} to charge C1.

III. SIMULATION RESULTS

Simulation results show the successful operation of the boost converter. Table I summarizes the overall characteristics. The maximum efficiency of the boost converter is 92 % at Vg = 5 V, VGH = 12 V, and load current = 120 mA. Fig. 6 illustrates output voltages according to variation in the load current. The test is conducted with Vg = 3 V, VGH = 10 V, inductor = 4.7 uH, capacitor = 4.7 uF, and a load current variation of 10 $\sim$ 100 $\sim$ 10 mA. Fig. 7 also illustrates output voltages according to variation in the load current. The test is conducted with Vg = 3 V, VGH = 20 V, inductor = 4.7 uH, capacitor = 4.7 uF, and a load current variation of 10 $\sim$ 100 $\sim$ 10 mA. As the simulation results indicate, the boost converter displays stable operation even under substantial load current variation. Fig. 8 shows the start-up operation of the boost converter. The test is conducted with Vg = 3 V, VGH = 10 V, inductor = 4.7 uH, capacitor = 4.7 uF. The efficiency of the boost converter is shown in Fig. 9.

IV. CONCLUSION

In this paper, the boost converter is designed using a 0.5 μm 5 V, 3.5 μm 30-V CMOS process for TFT-LCD bias

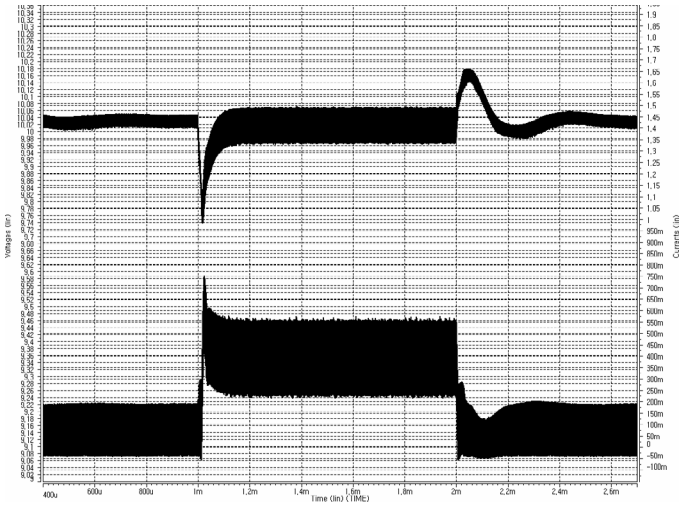

Fig. 6. Load transient response.(Vg=3V, VGH=10V)

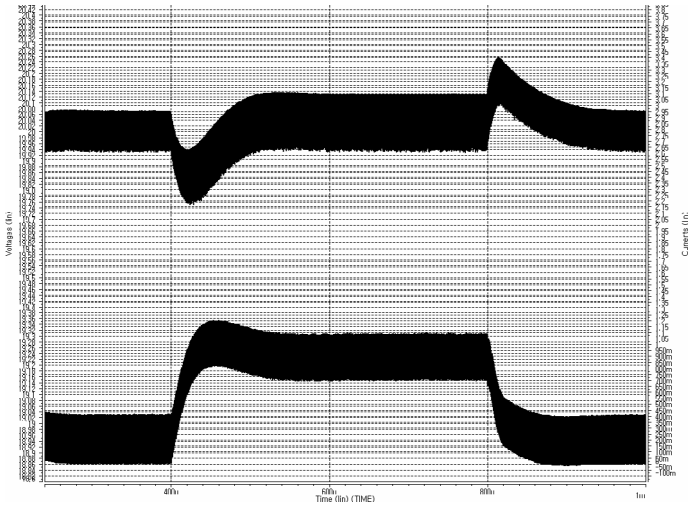

Fig. 7. Load transient response.(Vg=3V, VGH=20V)

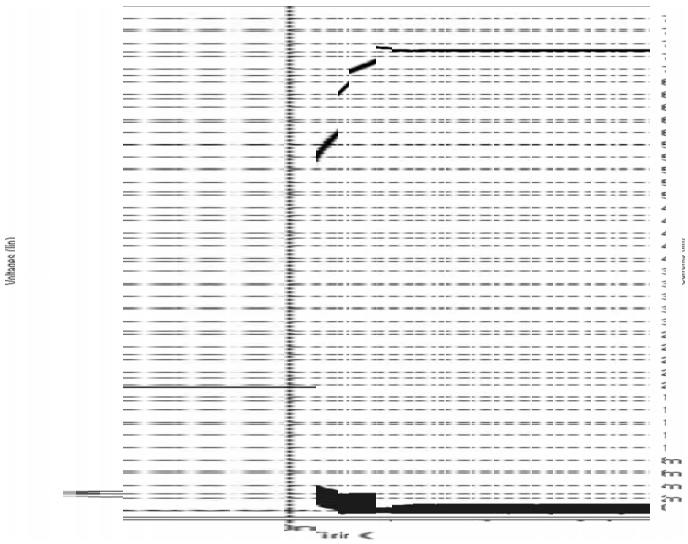

Fig. 8. Startup operation.

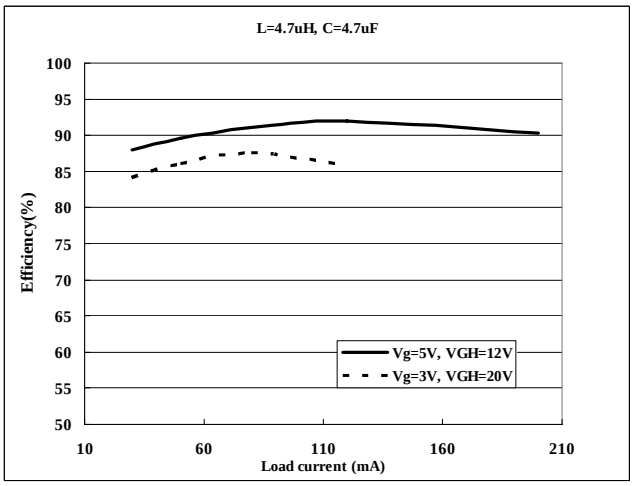

Fig. 9. Power conversion efficiency.

supply. Simulation results verify that the boost converter is accurately controlled by external resistors. The boost converter not only displays stable operation even under substantial load current variation but also provides power conversion efficiency higher than 90 %. The boost converter is capable of supplying optimized power for a wide range of systems, especially for TFT-LCD bias supply.

ACKNOWLEDGEMENT

This work was supported by the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea government (MEST) (No. R01-2008-000-11056-0).

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