A Level Shifter for a Bias-Offset Transconductor

Fujihiko Matsumoto, Toshio Miyazawa, Shintaro Nakamura and Yasuaki Noguchi
Department of Applied Physics, National Defense Academy
1-10-20, Hashirimizu, Yokosuka, Kanagawa, 239-8686, Japan
TEL:+81-46-841-3810 ext.3624 FAX:+81-46-844-5912(Dept.of Applied Physics)
E-mail : matsugen@nda.ac.jp(F.Matsumoto)

Abstract: A transconductor is a fundamental building block for analog signal processing circuits, such as filters and multipliers. For such applications, the transfer characteristic of the transconductor is desired to be linear. The bias-offset transconductor is known as a linear MOS transconductor. The transconductor has floating voltage sources. This paper presents a new design of the floating voltage source. If the proposed circuit is used as a level shifter for the linear transconductor, the output DC voltage is more accurate than that of the conventional circuit. Further, the proposed circuit is used as the second signal voltage source for a multiplier, the second harmonic distortion is improved. Simulation results show those advantages.

1. Introduction

A transconductor is a fundamental building block for analog signal processing circuits, such as filters and multipliers. For such applications, the transfer characteristic of the transconductor is required to be linear. A bias-offset circuit shown in Fig.1 is a linear MOS transconductor[1], [2]. This circuit has floating voltage sources V_B. Because the theoretical characteristics of the output current and the transconductance are proportional to V_B, the transfer characteristic can be tuned by V_B if V_B is set to DC voltage and is used as a level shifter. On the other hand, if V_B is used as the second AC signal source, this circuit can be used as a multiplier.

The authors have studied the compensation method for variation of the characteristic of a transconductor using the bias-offset technique. In considering a design of a control circuit for the characteristic compensation[3], [4], [5], the authors paid attention to the floating voltage sources to realize V_B. In order to maintain effective compensation regardless of changes of V_B or operating currents, combination of the control circuit and the floating voltage source has been examined. In this study, a new floating voltage source has been designed, which is compared with the conventional circuit[2]. The proposed circuit is used as a level shifter for a linear transconductor and used as a signal source for a multiplier. This paper reports the characteristic of the level shifter and the multiplier employing the level shifter.

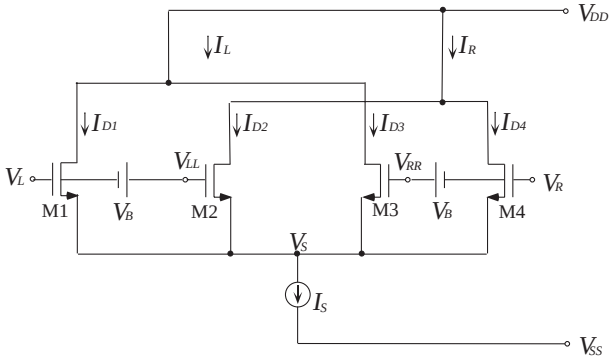

Figure 1. MOS transconductor using bias offset technique

2. MOS Transconductor using Bias-Offset Technique

Fig.1 shows the MOS transconductor using bias-offset technique. Assuming that a drain current I_D of an MOS transistor obeys the square-law characteristic, I_D of M1-M4 are expressed as

$$\begin{aligned} I_{D1} &= K_N(V_L - V_S - V_{TN})^2 \\ I_{D3} &= K_N(V_R - V_S - V_{TN})^2 \\ I_{D2} &= K_N(V_L - V_B - V_S - V_{TN})^2 \\ I_{D4} &= K_N(V_R - V_B - V_S - V_{TN})^2 \end{aligned} \tag{1}$$

where K_N is an ideal transconductance factor, V_{TN} is the threshold voltage, and V_S is common-source voltage of M1-M4, respectively. The output current I_{out} is expressed as

$$I_{out} = (I_{D1} - I_{D3}) - (I_{D2} - I_{D4}). \tag{2}$$

Assuming that the input voltage is a fully differential signal, the input voltage V_{in} is expressed as

$$\begin{aligned} V_{in} &= V_L - V_R \\ V_L + V_R &= 0. \end{aligned} \tag{3}$$

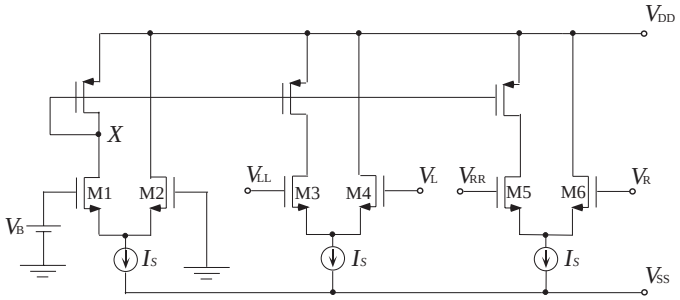

Figure 2. Conventional floating voltage source

From Eq.(1)–(3), the relation between the input voltage V_{in} and the output current I_{out} is expressed as

$$I_{out} = 2K_N V_B V_{in}. \tag{4}$$

The transeconductance G_m is expressed as

$$G_m = \frac{dI_{out}}{dV_{in}} = 2K_N V_B. \tag{5}$$

From Eq.(5), G_m is determined by the transconductance factor K_N of M1-M4 and the bias voltage V_B.

The conventional floating voltage source is shown in Fig.2[2]. If V_B is applied to the gate terminal of M1, the relation among the gate voltages of M6–M9, namely V_L, V_{LL}, V_R and V_{RR} are expressed as

$$V_{LL} - V_L = V_{RR} - V_R = V_B. \tag{6}$$

3. Proposed Circuit

The proposed circuit is shown in Fig.3. The differencial pair M1-M2 and the feedback circuit composed of M7 and M8 form the reference circuit, which corresponds to the differential pair M1-M2 in Fig.2. Copying the current of M8 to M9 and M10, the floating voltage between the gate terminals of M1 and M2 is reproduced between the gate terminals of M3 and M4, and those of M5 and M6.

The gate voltage of M7, namely the voltage at node X, is determined by the gate-source voltages of M7 and M8. If I_{SS} and/or I_t are changed, the gate-source voltages are also changed. Moreover, the drain-gate voltage of M1 depends on V_B. On the other hand, the drain-gate voltages of M3 and M5 are 0V. Thus, the operating state of M1 differs from those of M3 and M5. It is necessary to alleviate the difference of V_{DG} between M1 and the others for accurate floating voltage output. The part surrounded by the broken line is a coordination circuit to vary the voltage at the node X.

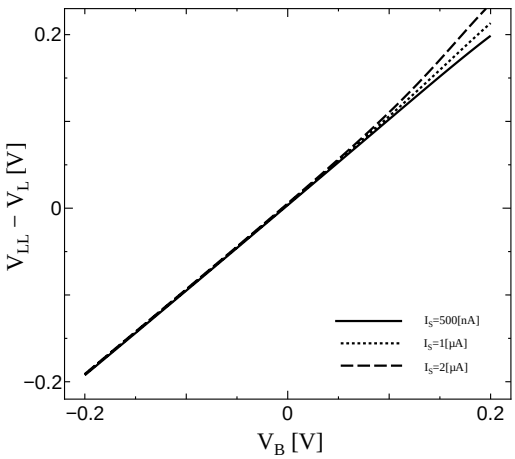

Figure 4. Relation between V_B and $V_{LL} - V_L$ of the conventional level shifter

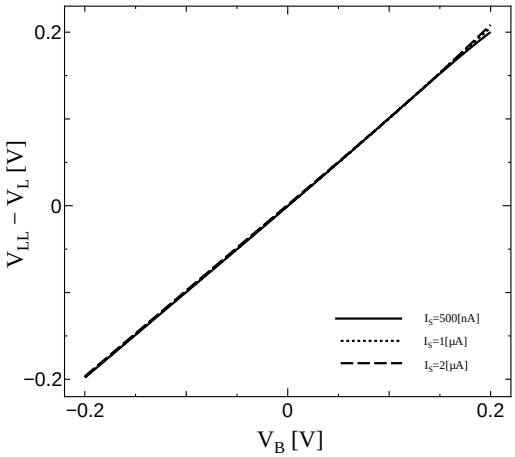

Figure 5. Relation between V_B and $V_{LL} - V_L$ of the proposed level shifter

4. Simulation

In order to confirm the validity of the proposed circuit, simulation was carried out. The used analysis program is SIMetrix. In simulation, 0.18[μm] BSIM3 Model is used. The applied voltage is ± 0.9[V].

4.1 Floating voltage of level shifter

Fig.4 and 5 illustrate the floating voltage between V_B and $V_{LL} - V_L$ of the conventional and the proposed circuits, which are used as level shifters. As shown in Eq.(6), the characteristic of both circuits are equal theoretically. The figures show that deviations of the proposed circuit due to variation of the operating current I_S

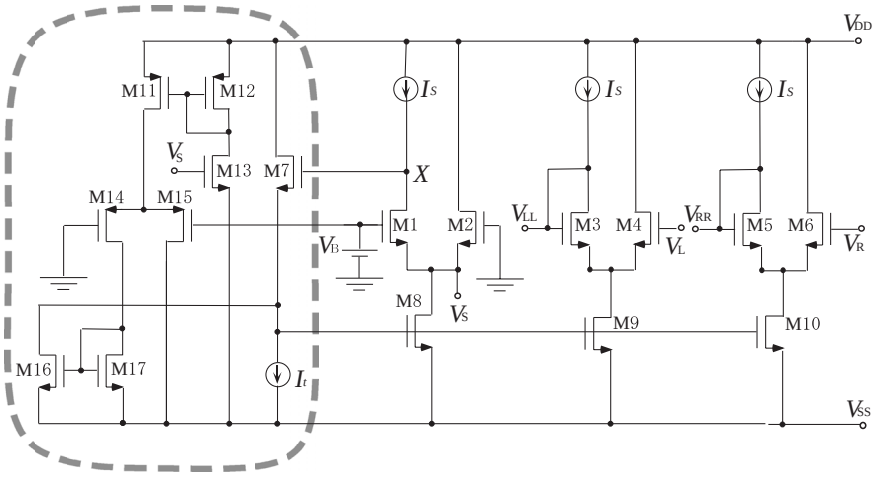

Figure 3. Proposed floating voltage source

is smaller than that of the conventional circuit.

4.2 Floating voltage for bias-offset transconductor

The level shifter is connected to the bias-offset transconductor, where V_B is constant. The relation between the input voltage of the transconductor V_{in} and $V_{LL} - V_L$ is illustrated in Fig.6 for $V_B = 0.1$V. Each operating currents I_S of the conventional and the proposed circuits are varied. The ideal characteristic must be that $V_{LL} - V_L = 0.1$ regardless of the input voltage of the transconductor. This means that the characteristic draws a horizontal line. The figure shows that the variation of $V_{LL} - V_L$ of the proposed circuit due to the change of the operating current is much smaller than that of the conventional circuit. Moreover, the value of $V_{LL} - V_L$ is close to 0.1V at $V_{in} = 0$V. It is considered that the coordination circuit performs effectively.

The relation between the input voltage of the transconductor V_{in} and $V_{LL} - V_L$ is illustrated in Fig.7 for $V_B = -0.1$V. The variations due to operating current of the conventional and the proposed circuits are in similar degree. Slopes of the curves of the proposed circuit are larger. However, the value of $V_{LL} - V_L$ is closer to -0.1V than the conventional one at $V_{in} = 0$V.

Fig.8 illustrates the transfer characteristics of the transconductor for V_B ± 0.025V, ± 0.05V and ± 0.1V. From Fig.8, it is confirmed that the circuit operates as a transconductor and a multiplier.

Finally, harmonic distortion of the multiplier, in which the proposed circuit is used as the second signal source, is discussed. The second and the third harmonic distortions (HD2 and HD3) are analyzed in case that V_{in} is 0.2V of DC. A sinusoid input voltage, whose amplitude is 0.1V, is applied as V_B. Table.1 and 2 show the results of HD2 and HD3 for 1kHz and 10kHz, respectively. Each Table also shows the results of $I_S = 0.5\mu$A and 1μA. Although improvement of HD3 is a little, HD2 is much improved. From Fig.6.and 7., the absolute values of $V_{LL} - V_L$ of the proposed circuit are closer to $|V_B|$ than the conventional ones. This is the reason why HD2 is improved.

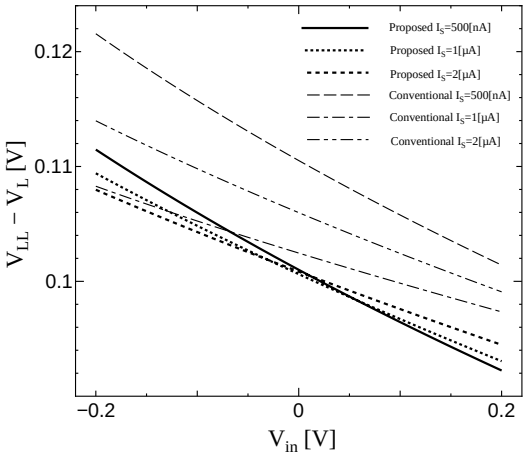

Figure 6. Relation between V_{in} and $V_{LL} - V_L$ for $V_B = 0.1$V

5. Conclusion

This paper has proposed a new circuit design of a floating voltage source for a bias offset transconductor. The proposed circuit is composed of a reference circuit, output circuits and a coordination circuit. Through simulation, the features of the proposed circuit have been con-

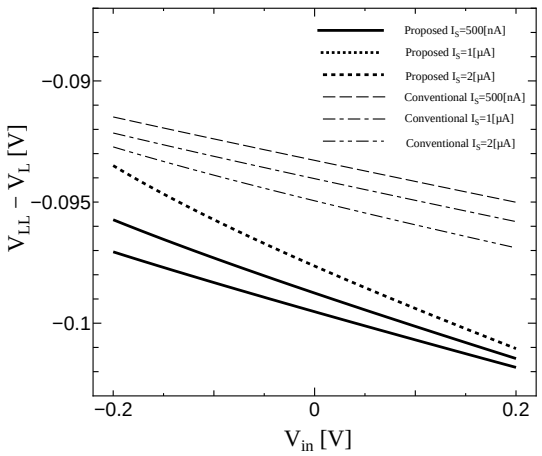

Figure 7. Relation between V_{in} and $V_{LL} - V_L$ for $V_B = -0.1$V

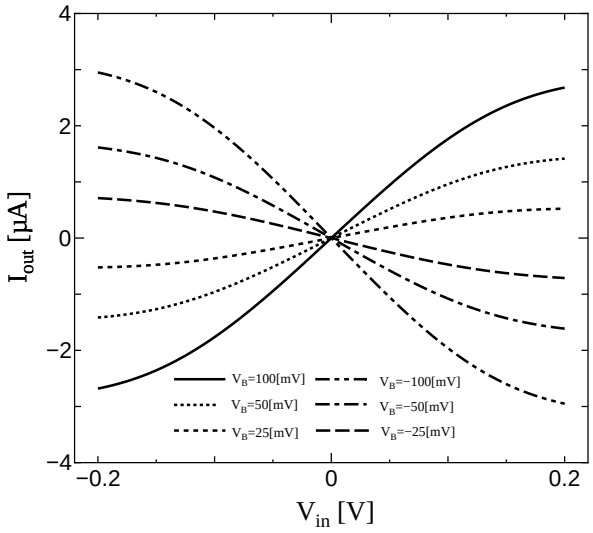

Figure 8. Transfer characteristics of the transconductor for ± 0.025V, ± 0.05V and ± 0.1V

firmed. It is found that the proposed circuit has higher accuracy of the output voltage and smaller variation due to the change of the operating current, in case that the proposed circuit is used as a level shifter. It also found that the second harmonic distortion is improved in case that the proposed circuit is used as a signal source of a multiplier. The future work is to realize the compensate system of characteristic variation of the transconductor employing the proposed circuit.

Table 1. 2nd and 3rd harmonic disctortion for 1kHz input voltage

$I_S = 0.5[\mu$A]	HD2[dB]	HD3[dB]
Proposed	-47.8	-28.0
Conventional	-39.8	-28.0
$I_S = 1.0[\mu$A]		
Proposed	-53.2	-33.2
Conventional	-39.8	-28.0

Table 2. 2nd and 3rd harmonic disctortion for 10kHz input voltage

$I_S = 0.5[\mu$A]	HD2[dB]	HD3[dB]
Proposed	-33.5	-29.8
Conventional	-27.4	-28.3
$I_S = 1.0[\mu$A]		
Proposed	-48.0	-33.9
Conventional	-33.2	-32.6

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