SOI devices - new challenges for Nano-Electronics

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The first reasons for the Silicon On Insulator (SOI) existence was the *radiations-hardened* circuits [1]. The targeted applications were those encountered in outer space, high-altitude flight, nuclear reactors, satellite communications, etc. The generated electron-hole pairs (GL) is proportional to the energy of the radiation.

Developing the SOI devices in alternative technologies (SIMOX, SOS, WB, UNIBOND), new applications become obviously, [2]. Novel and specific features of the SOI-MOSFETs are depicted in this Tutorials, two inversion channels commanded by two gates action, [3], "Kink" effect, Fully or Partially depleted structures, [2], applications in sensors and MEMS. The pseudo-MOS transistor is a special SOI device, without any photolithographic processes. Measurements and work regimes are presented. In situ, electrical characterization method based on the Pseudo-MOS technique is also included [4].

Nowadays, the SOI acronym must be reconsidered and generalized as *Semiconductors* On Insulators. The work principle of some SOI transistors with 200nm SiC films onto 400nm Si_3N_4 layer or Diamond On Insulator MOSFET were studied in previous work. The classical Organic-FET transistors are implemented in a default generalized SOI architecture, using the p-type Pentacene as Semiconductor on an insulator layer that can be SiO2 or polyimide. Few features of Organic-FET transistors simulated in Atlas/Silvaco are presented.

The nanodevices require an extremely thin semiconductor film as device body. To isolate this film is necessary to surround him by dielectric walls. Therefore, the SOI architecture still exists in more than 90% of the actual nano-devices, being the simplest and the natural way to implement a nano-device. The most representative nano-devices are discussed: SOI with volume inversion, Silicon On Nothing SON tranzistor, Few Electron Transistor FET, Single Electron Transistor SET, Nothing On Insulator NOI transistor.

An intensive investigated device in the lasts 10 years is Tunnel-FET, [5]. It has 50nm-Si horizontal p-i-n layer, placed on a buried oxide BOX of 100-50nm and is usually acted by the Back-Gate from this SOI configuration. The novelty is a Sub-threshold Slope SS of Tunnel-FET under 60mV/dec - the ideal physical limit of a conventional MOSFET.

The SOI association suggested few links for biomaterial extensions, like Biomaterials on Insulator, BOI, [6]. For instance, an epinephrine aqueous solution is a II-nd order conductor, with a conductance depending on the neurotransmitter concentration. The electrical properties are depicted. Another application concerns the bio-receptors immobilization on Si or SOI wafers in order to construct integrated biosensors. A typical application concern a glucose Bio-FET with a Glucose Oxidase GOX enzyme as receptor layer deposited on a Si-wafer. The TiO_2 nanostructured material was completely grown on the gate space, to offer a compatible inorganic support for the GOX enzyme. Integrated biosensors developed in SOI are discussed.

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