

A Design of Class-E Power Amplifier for Wireless Power Transfer System with Automatic Power Control Loop and Load Compensation Circuit

HyungGu Park ¹, Joon-Sung Park ¹, YoungGun Pu ¹, Yongnam Kim ²,
#Kang-Yoon Lee ¹

¹Department of Electronic Engineering, Konkuk University
Seoul, Korea, kylee@konkuk.ac.kr

²Unistream Co., Ltd.
Gyeonggi, Korea

Abstract

In this paper, class-E power amplifier (PA) with automatic power control loop and load compensation circuit is presented. The transmitted power is controlled by adjusting the signal applied to the gate of the power control transistor. In addition, a parallel capacitor is also controlled to enhance the efficiency and compensate for the load variation. This chip is implemented in a 0.35 μm BCD technology, and provides the output power control range of 10-30.2 dBm. The maximum power efficiency of the power amplifier is 71.5 %.

Keywords : Class-E Power Amplifier Power Control Load Compensation Wireless Power Transfer

1. Introduction

Currently the most power is consumed in power amplifiers for the use of mobile devices and wireless power transfer system. So it has become a very important circuit in terms of overall efficiency. Generally class-E power amplifier has the characteristics of high power efficiency but it still has a power consumption problem.

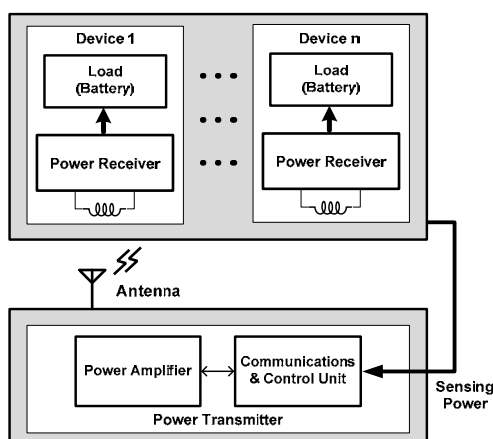


Figure 1: Block diagram of wireless power transfer system

A block diagram of wireless power transfer system is shown Figure 1. In order to increase the power efficiency, the power level is detected in the receiver and required power is supplied by the class-E power amplifier without maximum power transfer. In addition, it should be insensitive to the variation of the load.

This paper describes a class-E power amplifier with a power control technique by comparing reference voltage and output power level. In addition, load compensation circuit is based on a parallel capacitor that is also controlled to enhance the efficiency.

2. Architecture

In the receiver, the actual required power level can be varied by the variation of load or environmental factors. So transmit power must be controlled based on the detected receiver power. Moreover, the power efficiency should be compensated from variation of the load.

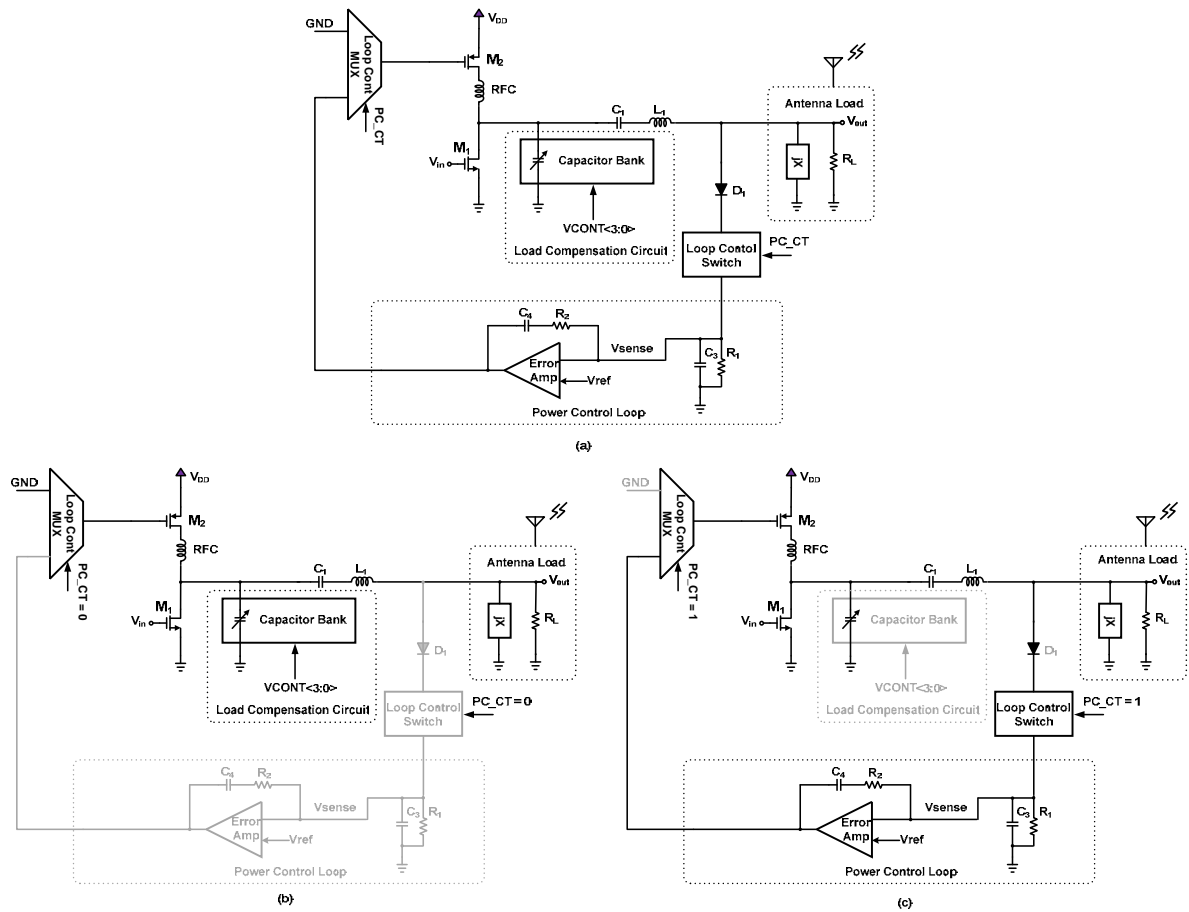


Figure 2: (a) Proposed schematic of class-E power amplifier; (b) load compensation mode; (c) automatic power control loop mode

The proposed structure for class-E amplifier is shown in Figure 2(a). Two steps for load compensation and automatic power control are as follows:

Step1 : The load compensation mode is shown in Figure 2(b). When PC_CT is '0', multiplexer outputs GND and the loop control switch is disabled. Then the change in output voltage due to load variation is detected by the load compensation circuit. And the parallel capacitor arrays are controlled by Vcont<3:0> so as to insensitize the power efficiency variation.

Step2 : The automatic power control loop mode is shown in Figure 2(c). The automatic power control loop is composed of the half wave rectifier and error amplifier. When PC_CT is '1', the loop control switch is enabled and error amplifier compares the feedback voltage, Vsense, with Vref, which is the current-sensing voltage from the receiver power. The error amplifier output controls the gate node of the M₂ and adjusts the supply current.

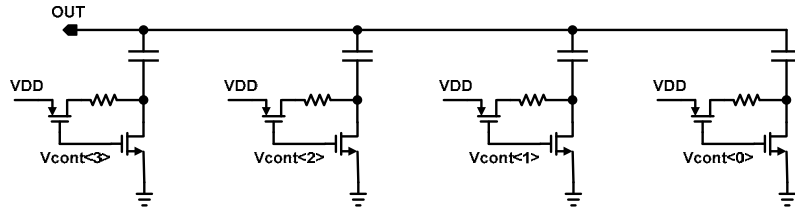


Figure 3: Schematic of capacitor bank

Figure 3 shows the schematic of capacitor bank. The capacitor bank consists of MIM capacitor and NMOS switches that are controlled by 4-bit, $V_{cont} \langle 3:0 \rangle$. When $V_{cont} \langle 3:0 \rangle$ go to high, NMOS switches are enabled. And the drain node of the NMOS is connected to VDD in order to prevent the floating node when $V_{cont} \langle 3:0 \rangle$ go to low.

3. Experimental Results

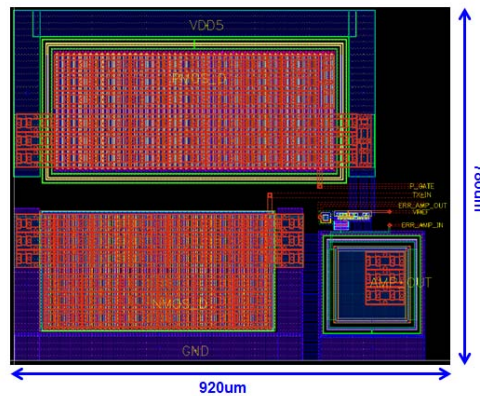


Figure 4: Layout of class-E power amplifier

The proposed class-E amplifier is fabricated using the $0.35 \mu\text{m}$ BCD CMOS process. Area is $0.92 \text{ mm} \times 0.78 \text{ mm}$ and supply voltage is 5 V . Layout of class-E power amplifier is shown Figure 4. We used the LDMOS(Laterally Diffusion Metal Oxide Semiconductor) to ensure the best performance in terms of linearity and efficiency.

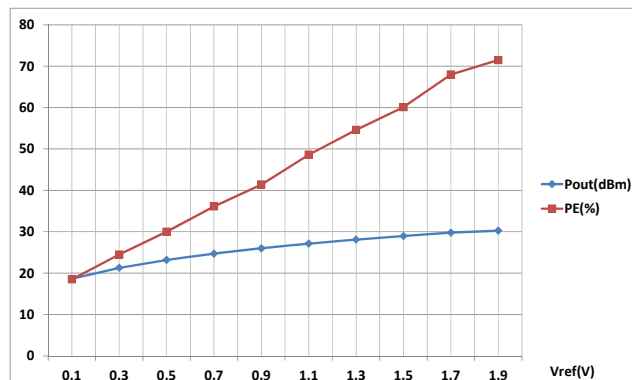


Figure 5: Performance of reference voltage vs output power and power efficiency

The simulated curve of reference voltage versus output power and power efficiency is shown in Figure 5. Maximum power efficiency is 71.5% and maximum output power is 30.2 dBm at reference voltage 1.8 V .

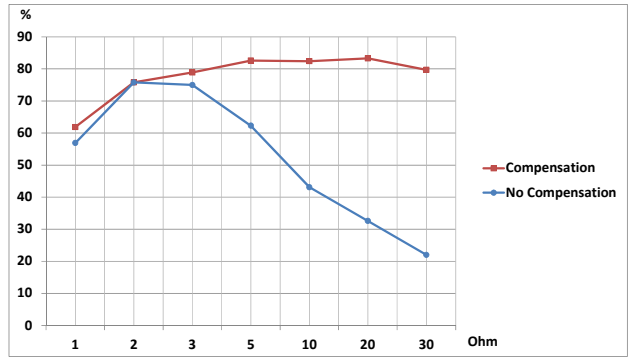


Figure 6: Characteristics of load compensation

The effect of load compensation on the power efficiency is shown Figure 6. Without the load compensation circuit, power efficiency would be degraded rapidly. When load compensation scheme is enable the power efficiency is insensitive to the load variation.

Table 1: Table of output power and power efficiency for tuning parallel capacitor

| Load (ohm) | Pout (dBm) | PE (%) | Tuning Capacitor (nF) |
|------------|------------|--------|-----------------------|
| 1 | 28.4 | 61.9 | 130 |
| 2 | 30.6 | 72.5 | 120 |
| 3 | 31.7 | 75.8 | 100 |
| 5 | 32.4 | 78.9 | 70 |
| 10 | 32.0 | 82.6 | 50 |
| 20 | 30.1 | 82.4 | 30 |
| 50 | 27.1 | 79.7 | 10 |

Table 1. shows the output power and power efficiency in tuning capacitor adjusted to variable load. It shows that parallel capacitor should be reduced to compensate for increasing the load.

4. Conclusion

In this paper, class-E power amplifier (PA) with automatic power control loop and load compensation circuit is presented. This chip is implemented in a 0.35 μm BCD technology, and provides the output power control range of 10-30.2 dBm. The maximum power efficiency of the power amplifier is 71.5 %.

References

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