77GHz CMOS Multi-Ranging Radar on a Chip (RoC)

[#]Cheonsoo Kim, Piljae Park, Dong-Young Kim*, Hyun Kyu Yu
Digital RF SoC Team, ETRI
*RF Conversion Component Team, ETRI
138 Gajeongro Yuseong Daejeon 305-350 Korea, cskim@etri.re.kr

Abstract

77GHz CMOS radar system development project have been progressing in ETRI from June 2010. In this work, a new radar architecture so called CMOS centric topology is proposed and transceiver blocks are implemented by 65nm CMOS technology. CMOS centric architecture employing eight channel I/Q modulated receivers with fully differential signal path and minimizing the millimetre-wave circuitry for signal handling difficulties, so all the beam-forming work is done at signal processing block, resulting in easy way to system on a CMOS chip or package. Furthermore, patch type array antenna also implemented in LTCC (Low Temperature Co-fired Ceramic) substrate and discuss about the performances of the radar on a package for small size, low cost and mass productive practical radar.

Keywords: 77GHz, CMOS, Multi-Radar, Chip, RoC

1. Introduction

Nano-CMOS technology has shown a good millimeter-wave band circuitry performance and to be a suitable way for cost-effective co-integration of RF transceiver and baseband signal process blocks [1-3]. Today's commercial 77GHz LRR(Long Range Radar) system, which consists of array antenna, multi-channel transceivers and baseband modules, costs relatively high to install not only luxury but to all compact cars [4]. In near future, the system also requires multi-ranging functions, as LR(Long Range) detection in 76-77 GHz band and SR(Short Range) detection in 77~81GHz band, with high angular resolution and long detection range concurrently [5]. For such a complicate multi-radar system, chip size and power dissipation is bottle neck for the system, so the architectural and technological innovation for the system design is essential and urgent.

To meet these needs, four year government financing project name of "Auto-motive Safety system Develop System based on CMOS Multi-Radar Sensors" have been starting at ETRI from June 2010. In this paper, we propose new CMOS radar architecture that is easy to co-integrate millimetre-wave front-end with base-band circuitry and signal processor. Furthermore, integration of small size patch array antenna with SoC will be also discussed in details.

2. 77GHz CMOS transceiver Design with 65nm CMOS Technology

2.1 CMOS Passive and Active Device Modelling up-to 110 GHz

Almost all the CMOS foundries support process design kit (PDK) modelled up to only 30GHz(see fig.1 and fig.2-(a)), and low inductance (<1nH) spiral inductor model, that is basic component in millimetre-wave circuits design, is deviate from EM simulation or measured results (see fig 2-(a)) in PDK because of the difficulties in low inductance measurement and de-embedding technique at millimeter wave range. Thus, the design of 77GHz CMOS radar transceiver chip is not easy and very risky work in current design environment. To solve these problems, we co-worked with GIT (Georgia Institute of Technology) for the topic of "Active/Passive CMOS modelling up to

110GHz for the application of auto-motive radar", and refined the equivalent circuit models of several active and passive components such as several widths of MOSFET and spiral inductors, transmission line, balun, DC block cap., by-pass cap., and so on. After the refined modelling work, whether it should be counted on circuit design or not, depends on the accuracy of modelling and accurate de-embedding procedure of active and passive device measurements [6-8].

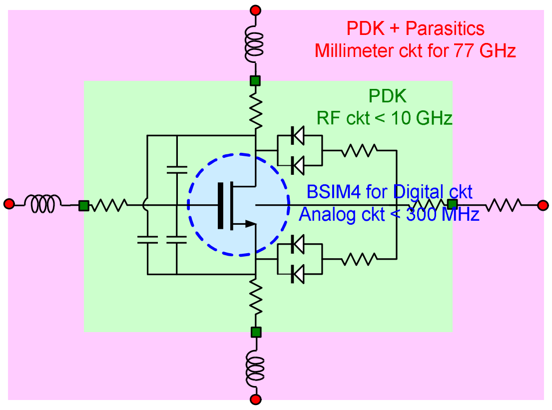

Figure.1 Equivalent circuit model of MOSFET when operating frequency change.

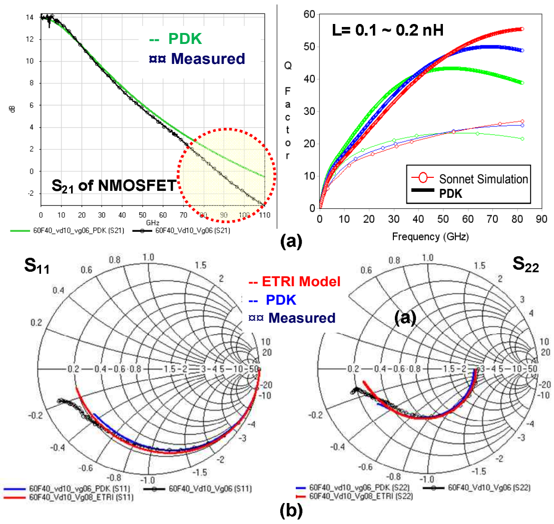

Figure.2 Comparison of measured and PDK performance: (a) NMOSFET with L=65nm, W=1.5um X 40, Quality factor of spiral inductor with inductance of 0.1~0.2 nH, (b) refined modelling results for S_{11}, S_{22} of NMOSFET with L=65nm, W=1.5um X 40 (at Vds=1.0V, Vgs=0.8V)

2.2 Design of 77GHz transceiver

New multi-ranging radar architecture, focused on a CMOS centric topology, is proposed as shown in Fig.3. It consists of eight receiver paths, two power amplifier and frequency generation block. Unlike the topology of the commercial chip, usually use phase shifting path at RF or LO path, the architecture consists of minimized millimetre-wave circuitry for its' difficulty of high frequency signal handling and I/Q receiver signal path with fully differential receiver topology for robust to localized noise and for improve the performance in multi-path reflections caused by multi-targets [5]. So the complicated phase shifting works are done at baseband processor block. For LRR and SRR detection at once, multi-slop frequency modulation (FMCW) scheme is adopted. The detailed circuit design and measured performance of each block will be shown and discuss at the conference.

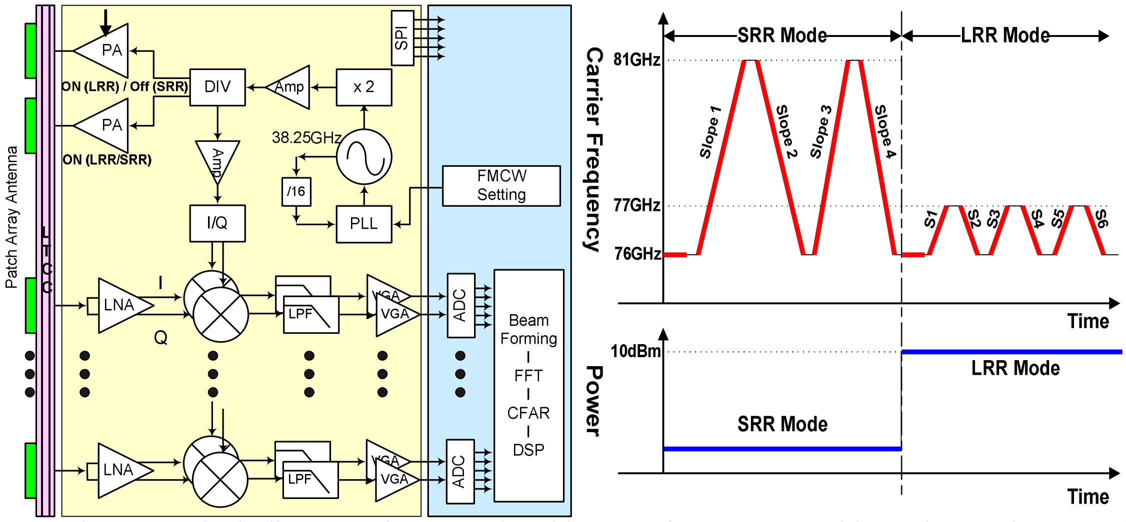

Figure 3: Block diagram of proposed architecture for CMOS Multi-ranging Radar on a chip, and FMCW modulation scheme for multi-targets LRR/SRR detection concurrently.

3. Array Patch Antenna Design for Small Radar on a Chip

The volume of commercial radar system is dominated by its antenna size due to the difficulties to obtain a high gain on substrate with high dielectric constant. Conventional patch array antenna fabricated in LTCC shows a low gain and efficiency because of the surface wave flowing at the surface, so a new array patch antenna structure employing the double resonator and 45^o polarization is proposed as shown in fig. 4. Simulated results of 12x1 arrays shows a high gain of 19dBi at 77GHz with the size of 40x8 mm^2.

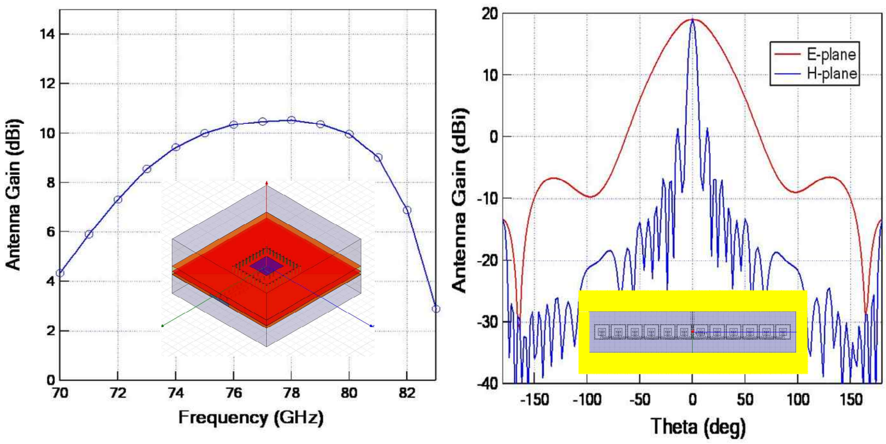

Figure 4: Simulated results of (single) and 12x1 arrays antenna depicts a high gain of (10.5), 19dBi at 77GHz with the size of 40x8 mm^2

4. Multi-Ranging Radar on a Small Package

The package cost of millimeter-wave IC and feeding cost of 77GHz array antenna with IC is another barrier to overcome for low cost radar system. The compatibility between the device and low cost assembly techniques like SMT (Surface Mounting technology) lead free processes is also a key factor of success for new generations of millimeter-wave devices [9]. Fig. 5 shows the recommendable co-integration structure for small size and low cost radar system. Patch array antenna is fed by transmission line and via in multi-layer LTCC, then connected to co-integrated RF transceiver and signal processor using flip chip technology using solder balls.

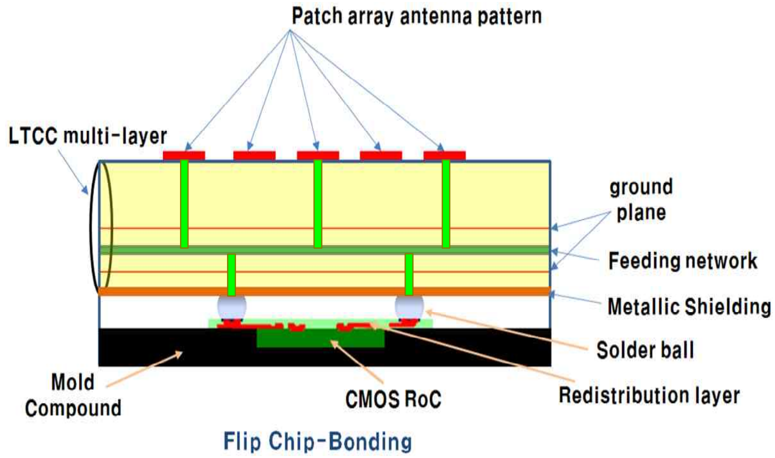

Figure 5: Cross-sectional view of proposed radar on a package structure for small size and low cost radar system.

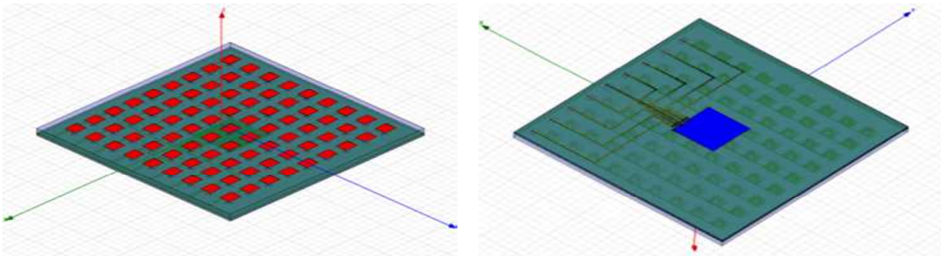

Figure 6: Top and bottom views of the proposed Radar on a Package structure.

Fig. 6 depicts the top and bottom views of the proposed Radar on a Package structure that is innovative and cost down to about more than one half compared with conventional radar system. It shows only patch array antenna at top view and single (or two) chips at bottom view on thin LTCC substrate at the size of below 5cm x 5cm. More detail explanations and experimental results will be discussed at the conference.

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