ADAPTIVE DIGITAL PREDISTORTION USING THE FPGA ELECTRONIC ARCHITECTURE

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ABSTRACT – Digital pre-distortion is an efficient means of compensating that can be help many engineering designers to control the power amplifiers non-linearity, using the *FPGA* electronic architectures as well as the adaptive *Look Up Table* implementation. Actually, many efforts of research have been done with the essential purpose to insert an efficient numerical algorithm in the hardware development. The main objective of this paper is to present a new way of how to develop algorithms using the numerical methods with the aid of the linear correlation as well as a linear regression. Thus, will turns out in a very great progress in the technique adopted applied to the adaptive pre-distortion linearization.

Index terms – Digital Pre-Distortion, Linearization, FPGA Architecture, Numerical Methods

1. INTRODUCTION

The adaptive pre-distortion of the modulated signals is a technique used to compensate distortions provoked by power amplifiers. Recently, many researcher centers have been using this technique due to the fact that it constitutes an efficient approach for a large class of *RF* models to control the intrinsic problems related with the non-linearity that appear in the implementation of many telecommunications systems. This technique has as one of its main fundamental principles to apply a distortion over the input signal with contrary effect to that one provoked by the amplifier, in order to obtain a linear answer of the system. As an additional convenience we can see an expressive reduction of the intermodulation products as well as the harmonic distortions that appear inside the band of the signal intrinsically.

Another alternative solution that we can set at the moment of the hardware implementation should be the reduction of the input power of the amplifier, in order to adjust the normal operation of the device over the linear region. Nowadays, this technique not have been using extensively just because it does not permit to explore all the potentially of the power amplifier, and it has a great consequence with respect to the cost of the transmission system [1] – [7].

2. PROGRAMMABLE LOGIC DEVICE

The electronic hardware we will present in this paper can be implement by using architectures like: *Programmable Logic Device* (*PLD*), which is a digital logic circuit that permits to implement a configuration including the *Programmable Logic Array* (*PAL*), *Field Programmable Gate Array* (*FPGA*) and the *Complex Programmable Logic Device* (*CPLD*).

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In our specific case we set the option to work with the *FPGA* structure since that this component has may convenience like: a very low cost, an easy programming and it demands a very simple manipulation. Besides of that, we can modify our project in any time without the necessity of to change the *chip*, which turns out in a very flexible component if we compare it with *Application Specific Integrated Circuit* (*ASIC*). Also we need to take into account that this device has an internal composition composed for segmented slide bars with metal composition, which crosses the chip in both vertical and horizontal directions and permit all connection in many alternative forms in accordance with all demanded requirements imposed over the project.

3. APPROACH DIGITAL PREDISTORTER

A very high efficiency and an expressive linearity are demanded when we are working with power amplifiers for TV signals. Due to the non-linear characteristics of these equipments we will make the use of linearization circuits by adopting the digital pre-distortion technique implemented using the as *FPGA*'s electronic architecture. Our project of the linearizator circuit will follow models, studied and research in accordance with [8] **–** [12].

Inside of the FPGA structure beyond the slide bars, it possess some *LUT*'s that can store the information to be transmitted, they permit to compare the transmitted signal with the feedback one and after that the data can be up to date at the *LUT*. If we taking into account both comparison and update approaches we can call the final hardware implementation an adaptive circuit, and in this case the best results have been gotten when we analyze the interrmodulation products of 3rd, 5th and 7th orders. Fig. 1(a) illustrates the block diagram of the implemented hardware, while the Fig. 1(b) depicts that one corresponding to the pre-distortion circuit.

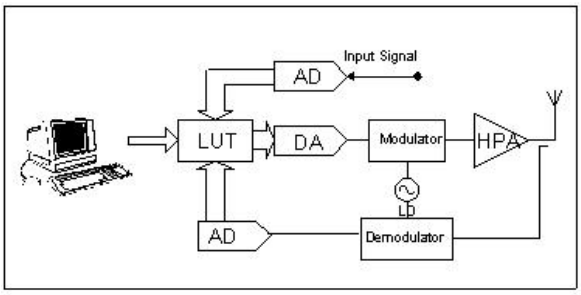

Figure 1(a) – Hardware Implementation.

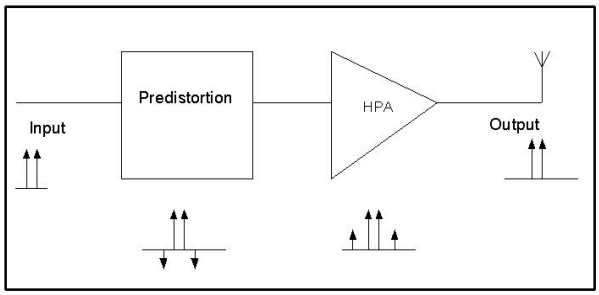

Figure 1(b) – Digital Pre-distortion Block Diagram.

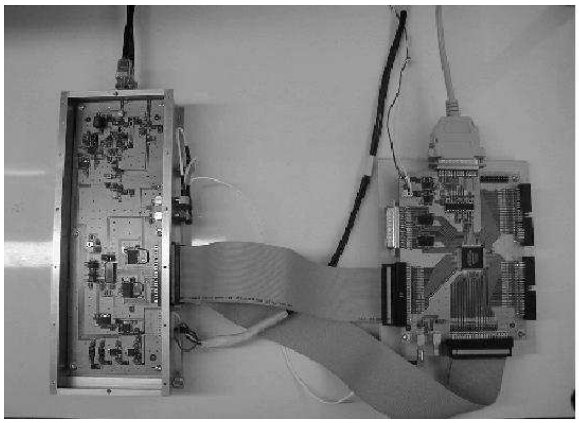

Figure 2(a) – Digital Pre-distortion Hardware.

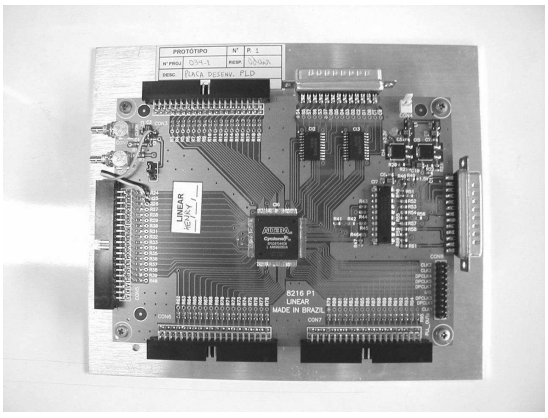

Figure 2(b) – *MLP* using the *FPGA*.

Our main proposal is to record in the *FPGA* a transference function contrary to that one generated by the power amplifier, and the imposition that we must to work with TV signals on real time demands that the correction must be very fast and with an adaptive process such that the user final does not perceive the intermediate operations. Fig. 2(a) presents a *Programmable Logic Module* (*MLP*) and the electronic implementation with both *AD* and DA converters, while in the Fig. 2(b) we only visualize the *MLP*.

4 – EXPERIMENTAL RESULTS THE LABORATORY

The results gotten with this hardware implementation are satisfactory and very important in the future system improvements, and it is easy to check that we correct the signal and it is possible to stay very close to that original one. The Figure 3 represent both input, amplifier, distorted and corrected signals in the time domain, while the Figure 4 illustrate the same signals in the frequency domain unless the amplifier signal that is in the time domain, as a comparison.

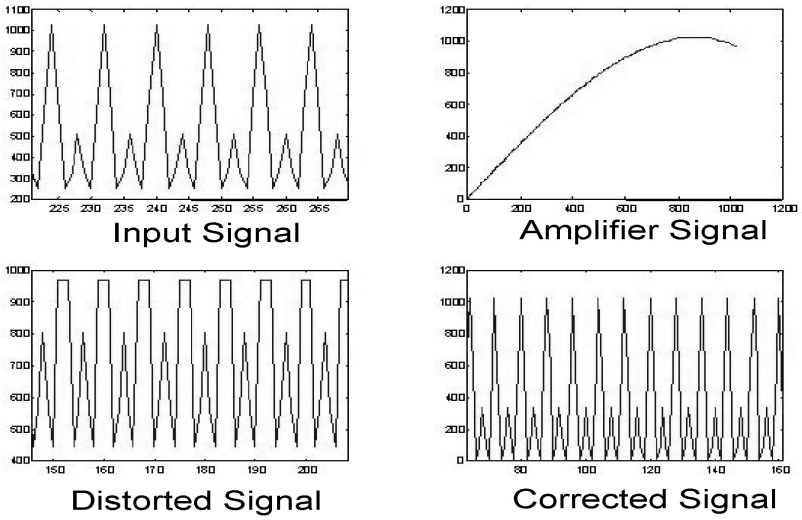

Figure 3 - Time Domain

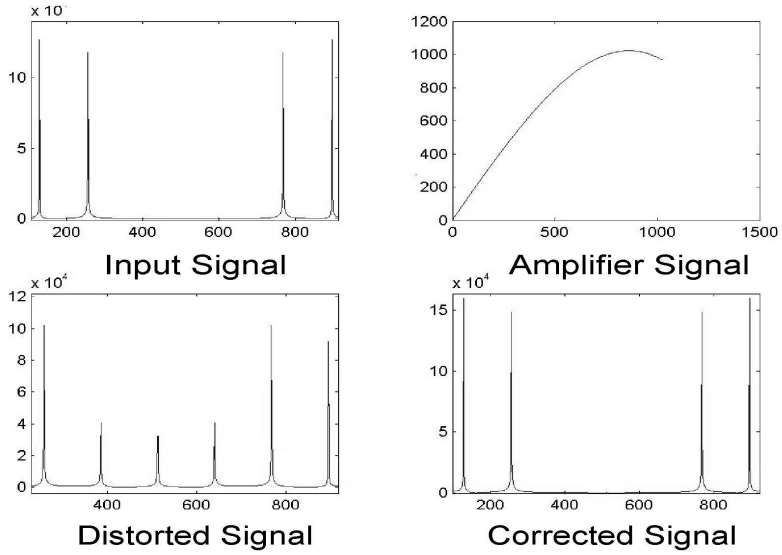

Figure 4 – Frequency Domain

These mentioned graphs had been made with the aid of the *MatLab* numerical platform, where after the simulation all data are recorded in the *FPGA*. Some classic laboratory instrument are used, like: oscilloscope, spectrum analyzer, etc. and we have gotten accurately the same curves that we have been simulated.

The input signal is a curve composed by two frequencies and after to pass for the amplifier, which has intrinsically no ideal performance the signal will distorted with the generation of harmonic components in the frequency domain and in consequence occurs some changes in its format in the time domain. By utilizing numerical methods over themselves it is possible to reestablish the original form of the input signal, which validates the linearization process we have adopted in this research and our developed technique [13] – [16].

4. CONCLUSION

This research permits to us to conclude that all laboratory activities have a great importance in the national marketing of broadcasting and indicates that is possible to increase the power efficiency of the system, making possible the reduction costs of the equipments. In addition, we can visualize more viable the digital *TV* signal transmission, independently of the pattern standard that each country will be adopt. The demanded requirements with respect to the power reduction and an expressive increase in the mistake tax provoked by the lack of linearity of the power amplifiers can be accomplished it we use the *FPGA´*s architectures that permit a easy way to set the numerical programming.

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