HIGH FREQUENCY PROPERTIES OF GaN BASED TRANSISTORS FOR MICROWAVE AND RF CONTROL APPLICATIONS

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Abstract

High frequency properties of AlGaN/GaN heterostructures field-effect transistors (HFET) used as control components for high-power microwave and RF control devices have been studied. A modified linear operation model was developed for these components so that electrical parameters may be determined as a function of frequency in better agreement with the experimental data. A model has been developed for the single shunt connected switch. From the model, it was established that the on-state low resistance and capacitance of the GaN switching HFET are frequency dependent. This phenomenon can have a dramatic impact on the control capabilities and design of microwave and RF control circuits using these devices. The modification of the two-terminal HFET model was implemented to compute the frequency dependence of the transistor impedance. Details of this modified GaN HFET switching model as well as simulation and measurement results are in this paper.

1. Introduction

Recent advances in semiconductor technologies based on wide bandgap materials such as GaN promise to extend the power level of FET-based microwave circuits by at least a factor of five due to their higher breakdown voltages [1-2]. The study of one of these structures, the HFET, for microwave and RF power control purposes is especially important because of their use in small size, high-density front end applications or in multifunction systems.

The low-power impedance frequency properties of field-effect transistors based on AlGaN/GaN heterostructure are studied. The first small-signal GaN HFET equivalent circuit studied [3-5] showed the impedance properties versus DC gate voltage control and transistor geometry, showing the relationship between gate length L_g and channel length L_{ch} for L_g less than L_{ch}. The second version of that model [5] described the impedance properties of transistors with shorter gate length compare with the channel length: L_g much less L_{ch}. These earlier model versions, however, do not adequately reflect the high frequency properties of the transistors that have been experimentally observed under low-power and high-power condition. The modified equivalent circuit is introduced in the paper and shows reasonable agreement with experimental data.

2. Distributed equivalent circuit

Figure 1 shows the structure of the AlGaN/GaN heterojunction field-effect transistor with the main network of resistors and capacitors forming the small-signal equivalent circuit. The two-dimensional electron gas (2DEG) located at the heterointerface is controllable only by the gate voltage of the device. Red marked elements of the network appear in the off-state, whereas the green elements only in the on-state, and the blue elements are present in both transistor states.

The source-drain resistance model corresponding to this network shows two n^+ regions under the source or drain and three regions in the heterointerface: directly under the gate and between gate-source and gate-drain. The value of the source and drain region resistors for the symmetrical transistor may be written as:

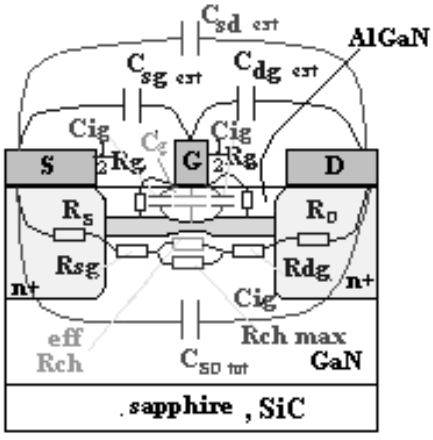

Fig.1 AlGaN/GaN HFET elements network

$$R_s = R_d = \frac{1}{\mu_n N\ q} \times \frac{L_{s(d)}}{W h_{n^+}}, \tag{1}$$

where μ_n is the low-field mobility, N is bulk impurity concentration in n^+ region, q is the electronic charge, W is the gate width of the HFET, h_{n+} is n^+ region depth, and $L_{s(d)}$ is the source (or drain) length. The 2DEG governs the resistance in the conductive channel, hence, the channel resistance may be written as:

$$R_{ch} = R_{sg} + R_{ch}^{eff*} + R_{dg}\,, \tag{2}$$

where R_{sg} and R_{sd} are the 2DEG source-gate and gate-drain resistance, and R_{ch}^{eff} is the channel resistance under the gate where the 2DEG sheet density is under direct DC gate voltage V_g control. The effective length L_{ch}^{eff} of this central part of the channel is:

$$L_{ch}^{eff} = (1 + \lambda_1) L_g\,, \tag{3}$$

where L_g is the gate length and λ_1 is a characteristic fitting coefficient taking into account the spreading of the DC electric field around the gate (λ_1 is typically between 0.05 and 0.25).

For a symmetrical transistor and zero voltage between source and drain ($V_{sd} \approx 0$) the source-gate or gate-drain resistances may be written as:

$$R_{sg} = R_{dg} = \frac{\left(L_{ch} - L_{ch}^{eff}\right)/2}{W} \times \frac{1}{q\mu_n n_s^{V_g=0}}\,, \tag{4}$$

where L_{ch} is the channel length (i.e. distanse between source and drain regions), and $n_s^{V_g=0}$ is the 2DEG sheet density under zero gate voltage condition and it is independent on the DC control gate voltage. The resistance corresponding to the area directly under the gate can be shown to be:

$$R_{ch}^{eff*} = \frac{R_{ch}^{eff}}{\left(1 + \left(R_{ch}^{eff} / R_{ch\max}\right)^{\gamma_2}\right)^{1/\gamma_2}}\,, \tag{5}$$

where $R_{ch}^{eff} = \frac{L_{ch}^{eff}}{W} \times \frac{1}{q\mu_n n_s(V_g)}$, $R_{ch\,\max} = \frac{1}{q\mu_{GaN} N_{GaN}} \times \frac{L_{g\,eff}}{W h_{GaN}}$, R_{ch}^{eff} is the 2DEG resistance under the gate, $n_s(V_g)$ is the gate voltage dependent 2DEG sheet density, $R_{ch\ max}$ is related to the bulk GaN resistivity under the gate region, h_{GaN} is the GaN thickness, N_{GaN} is the impurity level, and μ_{GaN} is the mobility in GaN. The parameter γ_2 is a characteristic parameter for the transition to reach the $R_{ch\ max}$ values and reflects the interaction between the bulk semiconductor and the quantum nature of the 2DEG. γ_2 was found to be approximately 0.3 [3]. Resistance R_g represents the resistance of the bulk AlGaN between the 2DEG layer and the gate. For a given HFET geometry, the depletion layer w_j caused by the gate Schottky barier exceeds the AlGaN layer thickness even for $V_g = 0$. We can estimate the resistor value as:

$$\begin{cases} R_g = R_{g\ \max} \approx 1...10\ MOhm, & for\ w_j \geq d_i \\ R_g = \frac{w_j}{d_i} \times R_{g\ \max} + \frac{1 - w_j}{d_i} \times R_{g\ \min}, & for\ 0 < w_j < d_i, \\ R_g = R_{g\ \min} = \frac{L_{g\ eff}}{W} \times \frac{1}{\mu_{AlGaN} N_D q}, & for\ w_j = 0 \end{cases} \tag{6}$$

where N_d is impurity level, μ_{AlGaN} is the mobility in AlGaN (in the first effort $\mu_{AlGaN} = \mu_n$), w_j is the depletion region under gate, $w_j = \sqrt{\frac{2\varepsilon_{AlGaN}}{qN_d}\left(V_{bi} - V_{th} - V_g\right)}$, ε_{AlGaN} is AlGaN dielectric permittivity, $\varepsilon_{Al_xGa_{1-x}N} = \varepsilon_{GaN} - (\varepsilon_{GaN} - \varepsilon_{AlN})x$, ε_{GaN} and ε_{AlN} are dielectric permittivity of GaN and AlN, respectively, x – the Al mole fraction in $Al_xGa_{1-x}N$.

The capacitance model includes both intrinsic and extrinsic capacitances. The extrinsic parasitic capacitance of the source and drain metal coupling to the gate metal in air (see Fig.1) is $C_{ext\,g}$. It is present in both transistor states. Parasitic extrinsic capacitance $C_{ext\,sd}$ couples the source and the drain above the semiconductor, and the intrinsic capacitance $C_{int\,sd}$ couples the same terminals through the semiconductor and substrate; it is present only in the non-conductive off-state, when the 2DEG is suppressed by the gate voltage. These capacitances are estimated using the standard expressions for MESFETs [6]. An extrinsic voltage dependent on-state capacitance between the higly conductive 2DEG and the gate C_g [7] and intrinsic off-state capacitance between gate and the inner sides of the 2DEG near source and drain C_{ig} [8] also exists. To compute these capacitaces, equations described in [3-5] were used.

The resulting equivalent circuit is shown in Fig.2. The capacitance C_{sd} reflects the total extrinsic and intrinsic capacitances between the source and drain. Resistors R_S and R_D are assumed small and are omitted in this model. The impedance Z_{gg} consists of a shunt connected gate resistor R_{gg} and parasitic capacitance C_{gg} to ground. Below we consider the situation when the drain is short-circuited to ground. R_{gg} has several origins and may include the inherent resistance of the gate material, or an intentionally added resistance to aid in keeping the gate floating above ground at high frequencies.

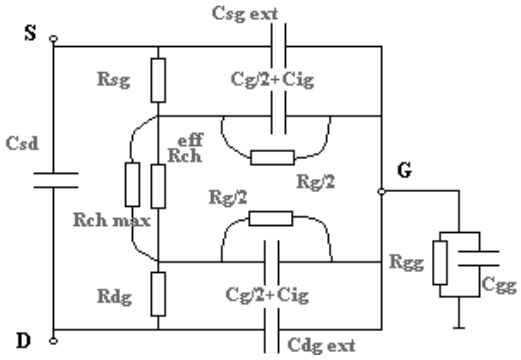

Fig.2 HFET equivalent circuit

3. Computed and measured results.

The device layer-structure parameters used for computer and experimental study are shown in Fig.3. The room temperature mobility of the 2DEG simulations was 545 cm^2/Vs^{-1}. The gate width used is 150 μm, the distance between the source and drain is 2 μm, and the gate length is 0.3 μm. Using the new modified equivalent circuit model, several general properties of the GaN HFET impedance

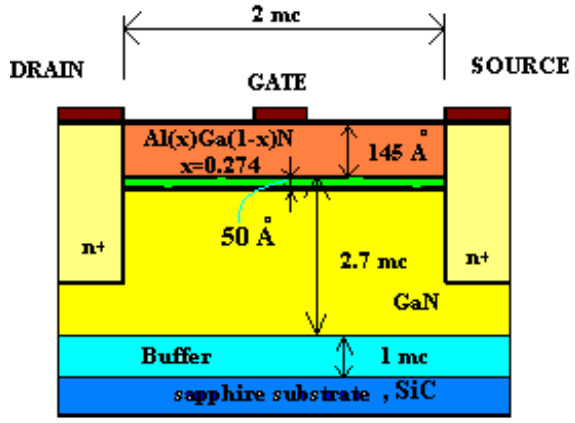

Fig.3 Layer structure of measured HFET

were computed versus frequency. Figures 4 and 5 show theoretical and experimental equivalent shunt resistance and shunt capacitance versus frequency at two gate biases (on and off-state).

Fig.4 shows simulated and measured high frequency properties of the on-state and off-state HFET resistances. Experiments showed an approximate 10% change with increasing frequency in the resistance at +2.0 volts on the gate over the frequency range 1 to 7 GHz. In the same frequency range the off-state resistance at –2 volts has changed about 25%. Fig.5 shows both simulated and experimental capacitance variations with frequency for both switch states. One can see about 40% change in measured on-state capaci-

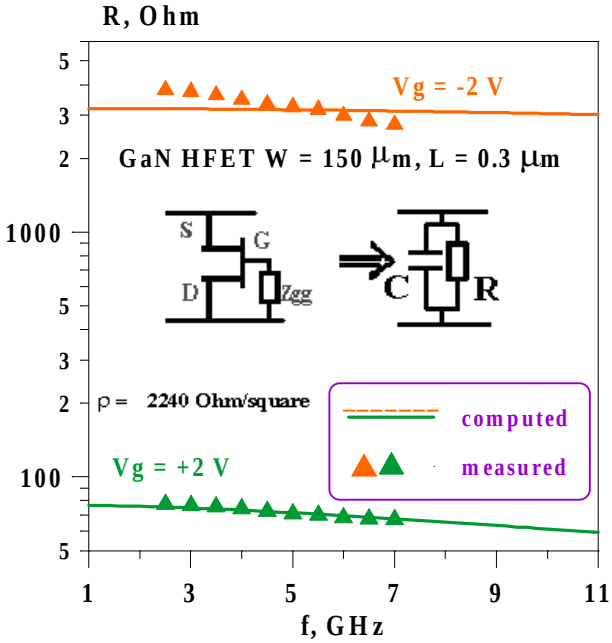

Fig.4 HFET resistance vs. frequency

tance and approximately 35% in measured off-state capacitance over the 1.0 to 7.0 GHz frequency range. The model shows better agreement for the on-state than for the off-state capacitance of the transistor. Fig.6 shows the simulated frequency response of shunt the switch's

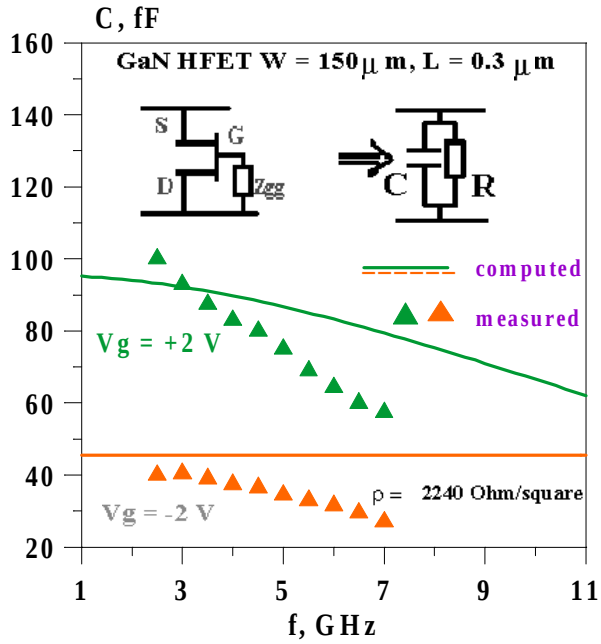

Fig.5 HFET resistance vs. frequency

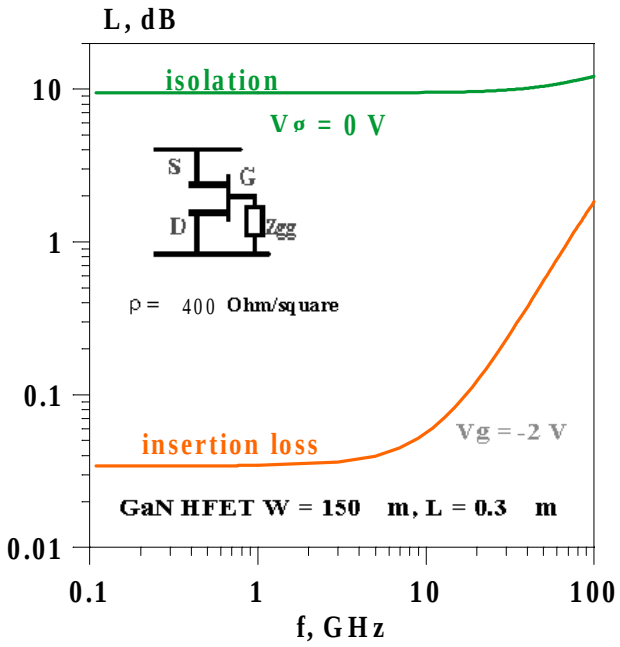

Fig.6 Simulated insertion loss and isolation

insertion loss and isolation computed for a sheet resistance of 400 Ω/ . There is little variation in either parameter with frequency below 2GHz while above this frequencya stronger dependence on frequency is observed for both parameters. This is due to the increased reactance from capacitances.

Conclusion

The focus of this paper is on the investigation into the frequency-dependent microwave and RF control impedance of HFET based on AlGaN/GaN. The investigation resulted in a modification of the current control two-terminal model into three-terminal to include the effects of the gate bias circuit. It was found that the largest variation in switch equivalent circuit parameters (resistance and capacitance) occurred in the on-state GaN HFET. The off-state device showed little variation in either parameter.

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