

A Non-Foster Circuit Design for Antenna Miniaturization

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Abstract - In this paper, a non-Foster circuit for achieving a negative small capacitance based on Linvill floating-type Negative Impedance Convertor (NIC) is realized. The effect of the parasitic elements and the transmission lines on the circuit performance is discussed. The experimental results show that the circuit presents a negative capacitor of 0.87pF in the UHF band. The circuit linearity test reveals a high output 1dB gain compression point at 7.8dBm and an output saturation point at 15.6dBm. Furthermore, the circuit has relatively high inter-modulation Output Intercept Points (OIPs).

Index Terms — Antenna miniaturization, Non-Foster circuit, Negative Impedance Convertor (NIC).

1. Introduction

Electrically Small Antennas (ESAs) are very attractive for emerging wireless technologies. However, antenna performance is bounded by some fundamental limits related to its size like Chu-McLean limit on the antenna Quality Factor (Q) [1]-[2] and Bode-Fano limit on its impedance bandwidth [3]. A possible solution for enhancing ESAs performance beyond these limits is the use of non-Foster matching [4]-[8]. This solution not only surpasses these limits [4] but also enhances antenna's performance in reception [5], improves its Noise Figure- (NF) [6] and its Signal to Noise Ratio- (SNR) compared to the same antenna without matching [7]. However, the design of non-Foster circuits is not an easy task and becomes more challenging when targeting at higher frequencies (due to the active components non-Linearity) and when targeting high impedance values (due to the parasitic elements). In this paper, we present a non-Foster circuit for ESAs matching. The circuit presents a negative capacitor of 0.87pF which is, up to the authors' knowledge, the smallest capacitance (the highest reactance) reported so far.

2. Non-Foster Circuit Design

Non-Foster circuits can be realized by using Negative Impedance Inverters (NIIs) or Negative Impedance Convertors (NICs). Looking into the available literature it can be seen that Linvill floating-type NIC (Fig. 1(a)) [9] is the most used topology. However, in practice the obtained impedance depends on the biasing conditions of the transistors. We started optimizing a Linvill floating type NIC to obtain a very small capacitance (very high reactance) in the UHF band. The active component is chosen to be BFR93A [10] because it is well suited for high frequencies (it has a transition frequency of $F_T=6\text{GHz}$). First, the transistor was modeled using its Spice parameters while the lumped components were

assumed to be ideal and no transmission line were included in the simulation. A prototype of the circuit was fabricated (Fig. 1(b)) and measured. The measured S parameters showed a significant divergence from the simulated ones as shown in Fig. 2(a). It should be noticed that the circuit is symmetric, hence, S_{11} and S_{22} are superimposed in simulation and the same for S_{12} and S_{21} . Then, a more realistic model of the circuit taking into account the parasitic elements of the transistor packaging, the lumped elements Q and self-resonance frequency and transmission lines corresponding to the circuit board, was simulated. The obtained results shown in Fig.2 (b) are in a very good agreement with the measured ones. The circuit is supplied by $5V_{DC}$, it consumes a current of 16.5mA or equivalently a DC power of 82.5mW. To have a stable circuit, the circuit overall reactance should be positive. Consequently, the circuit output is connected to a lumped network. The measured de-embedded reactance of this circuit is shown in Fig. 3(a). As it can be noticed, the reactance decreases with frequency which means that the circuit has a non-Foster behavior (it acts as a negative capacitance). The value of the equivalent capacitance is given in Fig. 3(b).

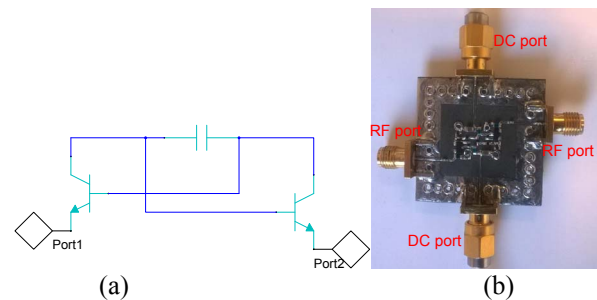


Fig. 1. The designed non-Foster circuit. (a) A general schematic of Linvill circuit and (b) the fabricated prototype.

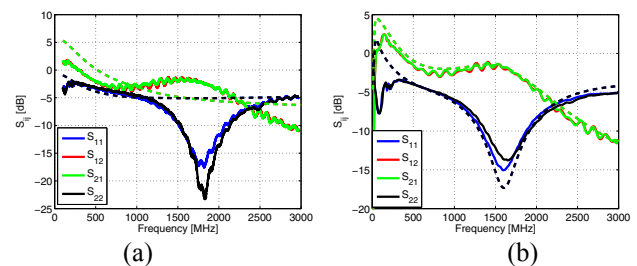


Fig. 2. A comparison between the simulated (dotted) and measured (continuous) S parameters of the designed circuit. (a) Considering ideal components and (b) realistic model.

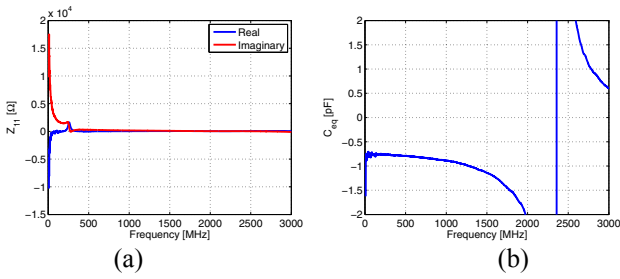


Fig. 3. Proposed NIC circuit measured parameters. (a) de-embedded input impedance and (b) equivalent capacitance.

The two-ports circuit S parameters were also used to study its stability using the different stability factors namely K, and μ . The obtained results are given in Fig. 4. Both factors show that the circuit is unconditionally stable starting from 1.5GHz. To investigate the stabilization possibilities of the circuit, its two ports stability circles were plotted in the unstable region at the following frequencies: (0.11, 1.31)GHz. The obtained results are given in Fig. 5, where for both cases the origin of the smith chart is in the stable region. As predicted by the results of μ factor, when the frequency increases, the stable region also increases. Furthermore, it can be noted that a capacitive load is required to stabilize the circuit, and hence, a monopole type antenna is a suitable choice.

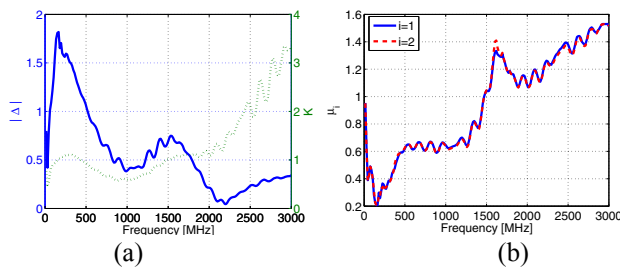


Fig. 4. Calculated stability factors of two-port NIC. (a) Roulette factor, and (b) μ .

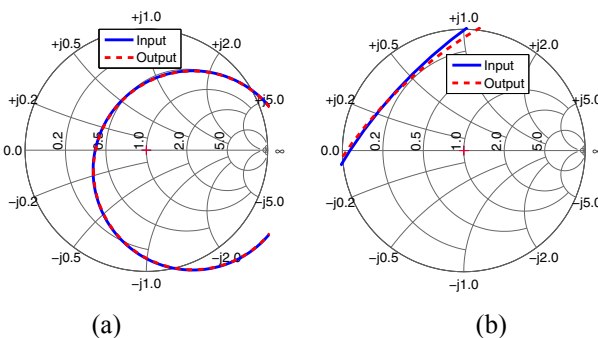


Fig. 5. Two-ports NIC stability circles at (a) 0.11GHz and (b) 1.31GHz.

The circuit was tested for the gain compression at 910MHz. The obtained results are given in Fig. 6. As it can be seen, the circuit has a high output 1dB gain compression point at 7.8dBm and an output saturation point at 15.6dBm. Later, the circuit was tested for two harmonics inter-modulation in the linear gain region. Two signal generators are used to generate two tones at 910MHz and 920MHz with an equal power changing from -20dBm to -10dBm to 0dBm. The circuit's first

two Output Intercept Points (OIPs) are $OIP_2=30\text{dBm}$ and $OIP_3=19\text{dBm}$. The circuit was also tested when the tones are at 910MHz and 911MHz revealing $OIP_2=28.2\text{dBm}$ and $OIP_3=17.7\text{dBm}$. These OIPs are in the average value of this type of circuits.

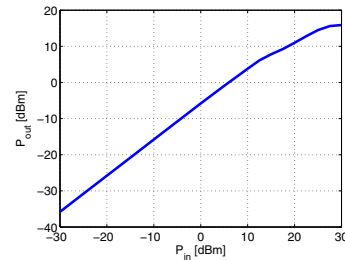


Fig. 6. Proposed NIC circuit measured parameters. (a) de-embedded input impedance and (b) equivalent capacitance.

3. Conclusion

In this paper, a non-Foster circuit for achieving a negative capacitor was designed. The effect of the parasitic elements and the transmission lines on the circuit performance was discussed. The circuit was fully characterized in terms of impedance, stability, linearity and inter-modulation. The performance of an electrically small Inverted-L Antenna (ILA) matched using the designed non-Foster circuit will be detailed during the conference.

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