FDTD ANALYSIS OF CPW-FED SLOT-ANTENNA COUPLING WITH MEMORY EFFICIENT PML BOUNDARY CONDITIONS

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Abstract

A full-wave analysis of transverse coupling between CPW-fed single-slot and twin-slot antenna elements at 60GHz is presented. Two single-slot elements separated by $\lambda_0/2$ on a $\lambda_d/4$ alumina substrate were coupled at $S_{21}=-30.2dB$. Two twin-slot antennas with the same separation had an S_{21} of -37.8dB, approximately 7.6dB less than that for the single slot case. Methods of reducing the TM_0 surface wave coupling are presented. A memory optimised implementation of the FDTD method with the PML Absorbing Boundary Condition (ABC) was used for the numerical analysis. Memory efficient application of the PML ABC is also discussed.

Introduction

Millimeter wave imaging systems have undergone rapid development in the past few years, partly due to maturing of millimeter wave technologies, potential application in automobile collision avoidance systems, airport security and all-weather landing systems. Several groups have researched quasi-optical power combining topologies and active antennas [1] in pursuit of high power and cost-effectiveness in such systems, the twin-slot coplanar waveguide (CPW) fed antenna has been proposed as a promising candidate for uniplanar millimeter wave imaging systems [2][4]. In an array environment, several problems must be addressed including feeding methods, optimal element separation, and crosstalk between neighboring elements.

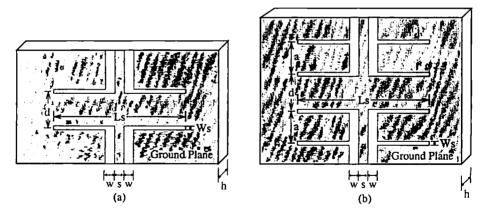


Figure 1: Single-slot and twin-slot test structures

Since CPW transmission lines are uniplanar, use of shunt lumped elements, active devices and compatability with HEMT fabrication processes are advantageous in design of millimeter wave systems. In addition, CPWs have lower radiation losses and less dispersion in comparison with microstrip transmission lines. In power combining or arrays with active devices, coupling between neighboring elements can cause low frequency oscillation and instability.

The purpose of this work is to analyse the coupling between two single-slot elements, and to present a method of reducing the coupling in an array. For all the analyses in this paper, a slot radiator of length $L_s = 2.0mm$ and width $W_s = 0.06mm$ was used. The slot length was chosen so that antenna works at second resonance to realise a broadband low impedance. With a substrate thickness of $\lambda_d/4$, surface wave losses are primarily due to the TM_0 substrate mode [4]. Coupling between twin-slot elements has been addressed by Laheurte et. al. [3] using moment methods, and Qian. et. al. [4] using the FDTD method. Laheurte et. al. performed an analysis on multilayered substrates with two CPW-fed slots operating in the even mode. By proper spacing of in-phase slots, it is possible to reduce coupling into the TM_0 mode due to phase cancellation of the substrate mode.

PML Implementation

The Finite Difference Time Domain [6] (FDTD) algorithm used supports conductive. and lossy materials. Termination of the simulation space is implemented via the Berenger's PML ABC [7]. In the current simulations, a reflection in the order of -55dB is achieved with an 8 layer PML, whereas a reflection of -30dB at best was obtained with Mur's 2nd order ABC [8].

Numerous papers have presented applications of the PML ABC and applied it to various structures to confirm it's validity. However, one continuing problem with application of the PML ABC is the large amounts of memory that are required. A standard PML "Yee Cell" consists of twelve field components, which should be of double precision (8 bytes) in order to realise better performance of the ABC. However, a standard Yee cell only consists of 6 field components, for which single precision (4 bytes) is sufficient. This difference in the architecture of Yee cells creates several problems in the application which must be considered. From a programming point of view, it is easier to define a simulation region which consists of 12 field components throughout. To the authors knowledge, most implementations of the Berenger PML have been of this type. A challenge lies in the implementation of a fast, memory efficient code.

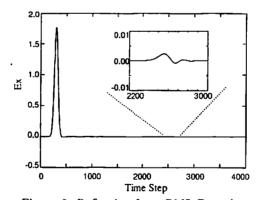


Figure 2: Reflection from PML Boundary

The implementation of PML that was used here, was coded in C. a high level language with provision for low-level memory handling functions. For the three dimensional case, the simulation region was subdivided into a $3 \times 3 \times 3$ array, which results in 27 separate regions of FDTD space. The central region consists of standard Yee cells and the outer regions consist of PML cells. Using this approach, a $100 \times 100 \times 100$ FDTD region, surrounded by a PML layer 8 cells thick, requires approximately 77.843×10^6 bytes, compared to 149.846×10^6 bytes for 12 field components throughout. This is about 48% less, allowing larger FDTD regions to be defined. For the case of a dielectric material penetrating into PML, it is necessary to include the effect of the dielectric on the PML conductivity profile. We have used constant multiplication arrays to calculate a constant for each material type, not for each field component in a trade-off against speed. In high performance RISC supercomputers with vector-addressing [9], indirect

addressing inside primary field update loops causes some overhead which is acceptable for some considering that memory is inevitably finite, whereas CPU time is not.

CPW-fed Slot Design

The CPW-fed single-slot antenna element in Fig. 1(a) has been analysed in a paper by Qian et. al. [5]. The CPW feedline apertures have a width w=0.030mm and a separation of s=0.120mm, resulting in a characteristic impedance of 42Ω at 60GHz. A single-slot element with a slot width $W_s=0.060mm$ and length $L_s=2.0mm$ on an alumina substrate $\varepsilon_r=10.0$ of thickness h=0.4mm will have an impedance of approximately 20Ω at 60GHz [5]. The single-slot by itself is not suitable for coupling to a the CPW feedline due to the impedance mismatch. Two slots in series will provide an effective impedance which is suited to the CPW feedline used. For the twin slot antenna in Fig. 1(b), the slots are separated by $a=2.1mm=\lambda_g$ at 60GHz. In such a configuration, the two slots are operating in the even mode. S_{11} for the twin-slot in an array is presented in Fig. 3. The minimum return loss is -19.3dB at 60.1GHz. It is slightly higher than the return loss of a single twin-slot element due to the loading effect and reflection from the second antenna.

Numerical analysis of coupling

For the numerical simulations, a PML thickness of 8 layers was used with $R(0) = 1.0 \times 10^{-5}$. This provided good results with a high dielectric constant substrate that was used. Excitation of the system was accomplished with a 3ps FWHM gaussian pulse, exciting the CPW feedline in the odd mode. 10 free space cells were used above and below the substrate. The potential in the CPW waveguide was recorded at each time step in a fixed location to obtain the transient response of the reflection and coupling between the slots.

CPW-fed single-slot coupling

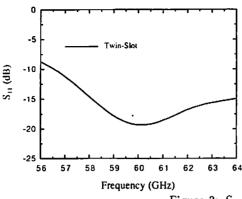
Numerical analysis of the single-slot was straightforward, with the definition of a simulation region of $102\delta x \times 30\delta y \times 110\delta z$, with $\delta x = 0.03mm$, $\delta y = 0.04mm$, $\delta z = 0.06mm$. The execution was stopped at 5000 time steps, which required approximately 90 minutes of CPU time on a single wide-node of an IBM SP2 supercomputer. A Fourier transform of the time domain response was carried out, and the S parameters extracted from the frequency domain data.

For the calculations, the single-slots were separated by 2.5mm which corresponds to $\lambda_0/2$ at 60GHz. The coupling between the antennas S_{21} is presented in Fig. 3. At 60GHz the coupling between the two single-slot antennas was -30.2dB.

CPW-fed twin-slot coupling

To analyse coupling for the twin-slot structure, a simulation region of $102\delta x \times 30\delta y \times 180\delta z$ was used, with $\delta x = 0.03mm$, $\delta y = 0.04mm$, $\delta z = 0.06mm$. The execution was stopped at 10000 time steps, which required approximately 300 minutes. The dimensions for the slot radiators, and the CPW feedline were identical to that for the single-slot case. Fig. 1(b) shows the structure that was analysed. The two slots were separated by $a = 2.1mm = \lambda_g$ at 60GHz. The end slots of the two twin-slot antennas were separated by d = 2.5mm. For the substrate used in these simulations, β/β_0 for the TM_0 substrate mode is 1.6 at 60GHz, therefore $\lambda_{TM_0} = 3.125mm$.

In order to achieve phase-cancellation of the TM_0 mode, the two slots should ideally be separated by $\lambda_{TM_0}/2$ which corresponds to 1.562mm. In the present configuration, the TM_0 substrate mode is approximately 242 degrees out of phase, which would theoretically result in less than optimal cancellation of the substrate modes. However, by choice of different substrate materials and adjustment of the CPW feeding line impedance, it should be possible to achieve a condition at which the slot separation s is equal to $\lambda_{TM_0}/2$ which would result in phase cancellation of the dominant TM_0 substrate mode.



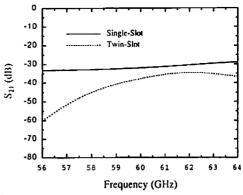


Figure 3: S_{11} and S_{21} parameters

For the twin-slot structure the coupling between the antennas, S_{21} was -37.8dB at 60GHz. The coupling between the twin-slot antennas, is 7.6dB less than that for the single-slot with the same antenna separation d. This result confirms the theory that the surface waves in this structure undergo phase cancellation. The coupling for the twin-slot antenna is significantly less than that of the single-slot antenna which permits tighter designs, and higher gain in active arrays.

Conclusion

We have investigated the implementation of the PML Boundary Condition for FDTD and discussed memory constraints of the method as well as methods for implementing the PML Boundary Condition with minimal memory requirements.

An analysis of the coupling between single-slot and twin-slot antennas in the transverse direction has been performed, with results indicating that coupling between two twin-slot antennas is less than the coupling between two single-slot antennas for the same antenna separation d. This is due to phase-cancellation of the TM_0 substrate mode, which in this structure is 242 degrees. Optimisation of the dielectric substrate should result in better cancellation of the substrate modes, and therefore allow closer element spacings in an array application.

References

- B. K. Kormanyos, W. Harokopus, L. P. B. Katehi, and G. M. Rebeiz, "CPW-Fed Active Slot Antennas", IEEE Trans. MTT., vol. 42, no. 4, pp. 541-545, Apr. 1994.
- [2] S. M. Wentworth, R. L. Rogers, J. G. Heston, D. P. Neikirk and T. Itoh, "Millimeter wave twin slot antennas on layered substrates", Int. J. Infrared Millimeter Waves, vol. 11, no. 2, pp. 111-131, 1990.
- [3] J. Laheurte, L. P. B. Katehi, and G. M. Rebeiz, "CPW-Fed Slot Antennas On Multilayered Dielectric Substrates", 24th European Microwave Conference, vol. 1, pp. 887-892, Sep. 1994.
- [4] Y. Qian and E. Yamashita, "All-Planar Millimeter wave Imaging Array(I) A New Imaging Element and Its Characteristics", *IEICE Tech. Report*, MW95-111, pp. 97-102, Nov. 1995.
- [5] Y. Qian and E. Yamashita, "All-Planar Millimeter wave Imaging Array(II) Design and Experiment of Single Imaging Element", IEICE Tech. Report, MW95-114, pp. 1-6, Dec. 1995.
- [6] K. S. Yee, "Numerical Solution of Initial Boundary Value Problems Involving Maxwells Equations in Isotropic Media", IEEE Trans. Ant. Prop., vol. AP-14, pp. 302-307, 1966.
- [7] J. P. Berenger, "A perfectly matched layer for the absorbtion of electromagnetic waves", J. Comput. Phys., vol. 114, no. 2, pp. 185-200, Oct. 1994.
- [8] G. Mur. "Absorbing boundary conditions for the finite-difference approximation of the time-domain electromagnetic field equations", IEEE Trans. Electromagn. Comput., vol. 23. pp. 377-382, Nov. 1981.
- [9] S. D. Gedney, "Finite-Difference Time-Domain Analysis of Microwave Circuit Devices on High Performance Vector/Parallel Computers", IEEE Trans. MTT, vol. 43, no. 10, pp. 2510-2514. Oct. 1995.