2010 International Symposium on Nonlinear Theory and its Applications
NOLTA2010, Krakow, Poland, September 5-8, 2010

Advanced PI/SI/EMI Simulation Technology for High-Speed Electronic Design

- Toward chip/package/board co-design -

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Abstract - With the progress of system integration technology, a variety of noise problems, so-called power/signal integrity and EMI issues, have become very serious in the field of chip (LSI), package and board (PCB) design.

These problems cause frequently the unexpected behaviors on the today's high-density and high-speed circuits. Thus, useful remedies are strongly demanded and the development of novel simulation technology has been expected for the short TAT (turn around time) and the cost reduction of a variety of high-performance electronic products.

In this report, the historical overview and the present status of the power/signal integrity problems and electrical simulation technology in the high-speed digital era are described. Furthermore, the future trend, including 3-dimensional and full-wave simulation techniques for PI/SI/EMI design, is suggested for the total solution of chip/package/board co-design.

1. Introduction

With the progress of circuit integration technology, the performance of electronic products has been improved drastically for these years. This fact has required much more skilful design because a variety of noise problems, which have not been considered previously, have become very serious. Noise issues are classified into 3 categories, namely, signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) [1-3].

In 1990's, discussions of SI problems such as time delay, reflection and cross talk have been started for the high-speed signal propagation on the interconnects. Furthermore, in 2000's, a variety of researches have been done actively for the analyses and the remedy for the PI and EMI problems such as simultaneous switching noise, ground bounce and radiation.

For the efficient design with consideration of SI/PI/EMI issues, simulation technologies get a lot of attention. Especially, novel electrical simulation technologies have been strongly demanded for the short TAT and the cost reduction, because these noise effects cause frequently unexpected behaviors and large damages on the high performance electronic products.

It is well-known that SPICE is conventionally one of the most useful tools to simulate the electrical behaviors[4], which is the lumped parameter circuit simulator. However, for more detailed verification of the high-density packaging and high-speed signals, the simulation should be done with the consideration of the 3-dimensional structures of interconnects, power/ground planes and so on.

In this report, first, today's problems in the chip/package/board co-design are summarized, and the present status and future trend of electrical simulation technology in high-speed digital era are described.

2. PI/SI/EMI and Chip/Package/Board Co-Design

2.1 What is high-speed signal ?

"High-speed" means that the signal includes high-frequency components. In such a case, we have to consider the circuit as a distributed parameter system, not as a lumped element system. When the length of the transmission line is long for the wave length of the signal, signal integrity becomes one of the most serious problems. Therefore, the line should be modeled by partial differential equations differently from the ordinary differential equations.

If the signal is sinusoidal wave, we need generally to regard the line as a transmission line in the case that the line length is longer than about 1/10 of the wave length. Therefore, for the signal of 1GHz, the line should be designed as a distributed parameter system when the line is longer than about 3[cm], namely, 1/10 of the wave length, $3*10^{10}$[cm]/10^{9}=30[cm]. Furthermore, for the line in the dielectrics, the length to be regarded as the distributed parameter system is shorter than 3[cm], since the velocity of electronic signal on the line is proportional to $1/\sqrt{\varepsilon}$, where ε is permittivity of dielectrics.

2.2 Chip/package/board co-design and PI/SI/EMI

Generally, LSI is fabricated on the silicon, and the chip is packaged and then it is mounted on the printed circuit board (PCB). In other words, circuit design is basically classified to 3 categories, namely, chip, package and board levels as shown in Fig.1.

The circuit design is categorized by analog and digital classes. However, with speedup (high frequency) of circuit operation, the boundary between analog and digital classes would be unclear and thus guarantee of signal quality (signal integrity) is also required for digital signals as well as analog ones.

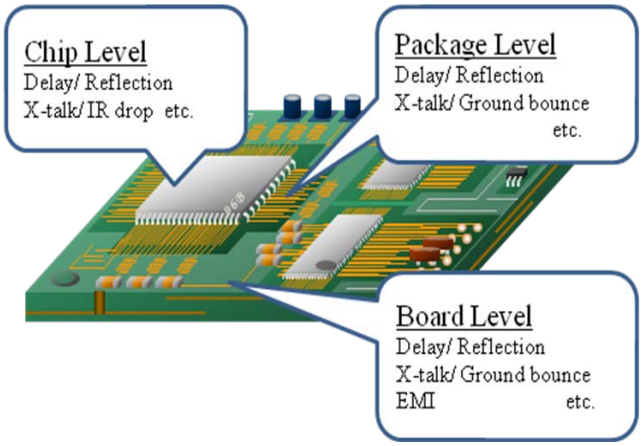

Fig.1 Power/signal integrity problems.

In 1980's, noise problem of IC was corresponding to the signal time-delay in the transistor. However, currently, signal propagation on interconnects is much larger problem. Furthermore, according to miniaturization of the circuit, a variety of noises, namely, reflection, cross-talk and IR drop became serious at the chip level. At the package and board levels, ground bounce such as SSN (simultaneous switching noise) is a very serious problem in the high-speed signaling because power/ground lines (planes) are connected each other in the system which is composed of chip, package and board. In order to complete the efficient design for the total system, advanced simulation technology, which can simulate the system in a body, is strongly demanded.

At the board design, typically, the line width is 50-100 [um], and 20-30 [um] at the package design. On the other hand, it is several dozen [nm] at the chip level. These scale differences raise a very serious problem in the 3-D physical simulation of the chip/package/board co-design,. Currently, we have no practical tools to simulate the system in a body. In order to reduce the simulation cost, a variety of macro-modeling methods have been proposed [5-6]. However, usually, some kinds of approximation techniques are used in these methods, thus novel physical simulation methodologies are expected for the detailed verification.

For higher frequency, modeling should be done by using Maxwell's equations based on electromagnetic theory, and 2-D and 3-D physical simulations should be done. Consequently, in order to simulate exactly the electrical behaviors, hybrid modeling and simulation based on lumped element, distributed parameter systems and electromagnetic theory are required.

In future, LSI-CAD (Computer-Aided Design)/CAE (Computer-Aided Engineering) will be combined with EMC-CAD/CAE. As a result, multi-level simulator should be developed. Furthermore, CAD/CAE system evolves to multi-physic CAD/CAE, which includes a variety of fields, namely, not only LSI and EMC but also thermal and mechanical fields and so on.

3. A Variety of Electrical Expressions

In the multi-level simulator as described above, a variety of electrical expressions are required as shown in Fig.2. Electronic circuits are classified into digital circuits and analog ones. A digital circuit is described by a set of logic functions (Boolean algebra) and an RLC lumped-element analog circuit in which many transistors are also included is formulated by a system of ordinary differential equations (ODEs). Because this type of circuit behaviors can be expressed reasonably as lumped-element circuit equations according to Kirchhoff's law, these formulations are suitable for the consideration of analog behaviors.

On the other hand, the lines (interconnects) should be modeled as the partial differential equations (PDEs) when they must be treated as transmission lines. Furthermore, expressions based on the Maxwell's equations are frequently required at the packaging/mounting level since the issues of power integrity and EMI are regarded as electromagnetic field problems in the high frequency domain.

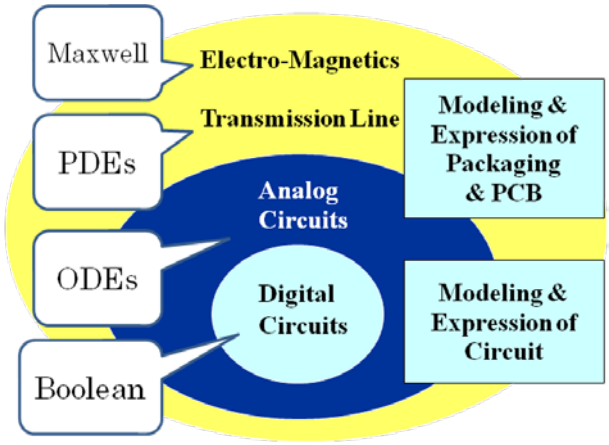

Fig.2 A variety of electrical expressions.

Because the total calculation cost has the trade-off for the simulation accuracy that is severely dependent on the modeling method, modeling and expressions such as ODEs, PDEs and Maxwell's equations have to be selected comprehensively. Furthermore, we have to use each of them skillfully and appropriately.

4. What Can Spice Do and Not Do?

SPICE (Simulation Program with Integrated Circuit Emphasis)-like circuit simulator for lumped parameter system has been widely used conventionally as a tool for signal integrity analysis of electronic circuits. By using SPICE, DC analysis, AC analysis and transient analysis of a circuit can be done. Although SPICE is effective for timing analysis of an electronic circuit, it spends usually an enormous calculation cost for the transient analysis of the large-scale network because it uses matrix solver.

In the design of high-frequency signaling, circuits must be simulated including the behaviors of interconnects precisely. SPICE possesses transmission line models and a variety of noises on interconnects can be simulated. For these years, power integrity (PI) problem such as ground bounce caused by simultaneous switching noise in the digital part is also serious. For the PI problems, the ground has to be modeled precisely for the exact simulation because the ground line and plane themselves fluctuate [1][3]. In other words, a ground plane must be modeled as 2- or 3-dimensional structure which is composed of a large number of passive RLCG elements. However, a netlist of SPICE becomes enormous and the calculation cost becomes impractical if the ground is modeled in detail. Therefore, some kind or another remedy for this problem is required.

As one of the remedies, model order reduction (MOR) techniques have been studied [5-6]. In MOR-based simulation methods, the large linear part is modeled as an equivalent and small macro-model. As a result, total simulation cost can be reduced drastically. These techniques are available for not only the MNA (Modified Nodal Approach)-based simulations but also electromagnetic field simulations[7]. However, these methods exploit some kind of approximation and are not efficient for the network with lots of ports. Thus, new strategies are strongly demanded.

5. Future Trend and Next Generation Simulators

In this section, recent some results of acceleration techniques are described for large-scale circuit simulations.

5.1 Fast circuit simulation methods

It is well-known that a class of relaxation method is available for the large-scale circuit simulation and a variety of techniques have been proposed in 1980's [8-9]. Furthermore, the LIM (Latency Insertion Method), which adopts a leap-frog algorithm which is used in FDTD (Finite-Difference Time-Domain[10]) method, has been proposed for the efficient simulation of large-scale RLGC networks[11], and it has been also shown that this method is suitable for the parallel-distributed simulation [12] and the multi-rate latency technique can be exploited[13]. After that, the implementation on the cloud computing system and the GPU (Graphics Processing Unit) has been done. Parallel-distributed LIM on the cloud computing system composed of 32 CPUs can be about 25 times faster than the original LIM[14]. LIM on CUDA with GPU (Geforce GTX295 composed of 240 streaming processors) is more than 30 times faster than the original LIM on the single CPU (Intel Xeon 3.2GHz)[15]. Although LIM is much faster than SPICE-like method, it is not directly applicable to the strongly coupled multi-conductor transmission lines. In order to cope with this problem, block LIM has been proposed [16], and the parallel-distributed block LIM has been also suggested [17]. Block LIM was used for the fast circuit simulator, SPIDER, as shown in Fig.3.

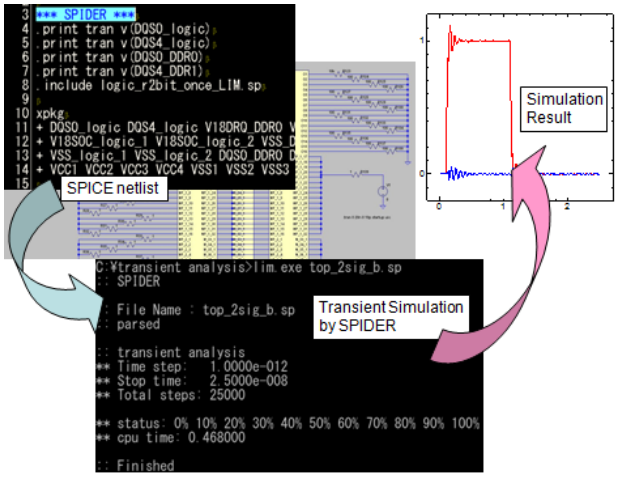

Fig.3 Fast circuit simulator SPIDER.

5.2 Fast electromagnetic simulation methods

For these years, 3D electromagnetic simulation methods have been studied for power integrity and EMI issues. FDTD method is simple and suitable for parallel-distributed calculations, thus 3D EMI simulator, BLESS, has been developed for the board design and estimation, through the collaboration between Shizuoka University and SONY, and sufficiently used for the practical PCB design [17]. Furthermore, GPGPU-based FDTD method has been also studied [18], where it is reported that GPGPU-FDTD is about 30 times faster than the conventional FDTD method with single CPU.

FDTD method is a very useful numerical simulation technique, but Courant-Friedrich-Levy (CFL) condition must be satisfied when this method is used, that is to say, the maximum time-step size is limited by the minimum cell size in the simulation

domain. In order to avoid the constraints from CFL condition, various implicit FDTD methods such as ADI (Alternating-Direction Implicit) -FDTD and HIE (Hybrid Implicit-Explicit) -FDTD methods have been proposed [20-21]. We have also proposed the alternating direction explicit (ADE) FDTD method [22-23], and the 3-dimensional EMI simulator has been developed as shown in Fig.4.

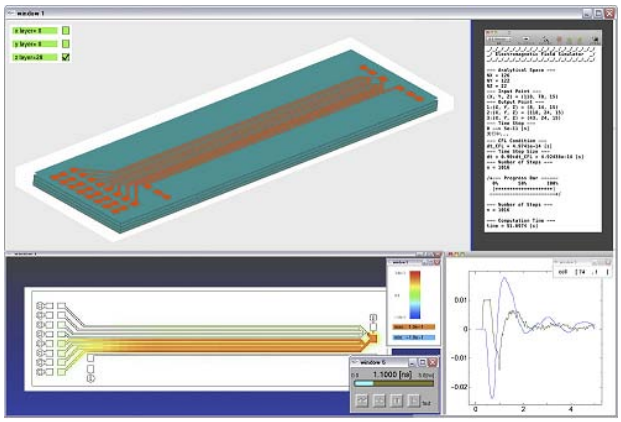

Fig.4 3D electromagnetic simulator.

6. Conclusions

In this report, the historical overview and the present status of the power/signal integrity verification methods have been described. Furthermore, the future trend and the next generation techniques, including 3-dimensional and full-wave techniques, have been suggested for the total solution of chip/package/board co-design.

In future, development of a multi-level simulator for SI/PI/EMI verification is expected for chip/package/board co-design.

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