Noise cancellation techniques used in CMOS low noise amplifiers

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Abstract—**CMOS low noise amplifiers represent the first active RF block on the receiver chain. Therefore, achieving low noise figure is of utmost importance. Event though the current CMOS amplifiers are optimized from the noise perspective, their noise figure still can be minimized by applying different compensation techniques. Based on an exhaustive literature, this article focuses on the noise cancellation principle, trying to offer some insight in designing low noise amplifiers with noise cancelling.**

Keywords- CMOS; LNA; noise cancellation; RF front-end

I. INTRODUCTION

The MOS transistor is recognized to have two noise sources:

a) flicker noise (or 1/f), caused by the charge carriers trapped at the interface between oxide and silicon and modeled as a voltage source in series with the gate;

b) thermal noise, associated to the resistive channel and modeled as a current source in parallel between drain and source.

Both noise sources are illustrated in Fig. 1 for an NMOS transistor. The thermal current noise can be approximated as $I_n^2(f) \approx 4kT\gamma g_m$ for long channel devices, where k is the Boltzmann constant, T is temperature in Kelvin, $g_{ds0} = g_{ds}\big|_{V_{DS}=0} \approx g_m$ while γ is 1 for linear region and 2/3 in saturation. In addition, it can be input-referred only, in which case the input voltage noise becomes $V_n^2(f) = \frac{4kT\gamma}{g_m}$.

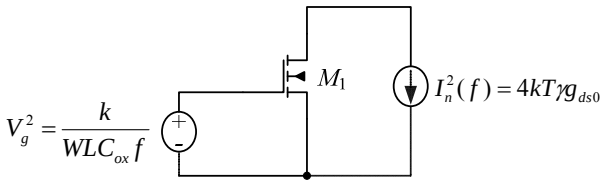

Figure 1. Sources of noise for MOS transistors.

Contrary to flicker noise whose influence decreases with frequency, the thermal noise becomes more significant as the frequency increases. This is the reason why the amplifiers envisaging higher frequencies (e.g. GHz applications) must be carefully designed from the noise perspective, the thermal noise being the major issue for RF/microwave amplifiers. Gain and noise are strong related each other at high frequencies, any decrease of gain causing a corresponding noise increase. As a major effect, the noise increase decreases the receiver sensitivity, therefore compensating the noise is in fact the first task when designing an RF front-end.

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II. INTERNAL NOISE COMPENSATION

Before presenting the cancellation principle, as proposed in the literature, it is important to clarify the concept of noise compensation. In this regard, it must be mentioned that the antenna receives not only the desired (deterministic) signals but also noise signals such as cosmic noise from stars or terrestrial background noise. And the main problem with the input noise is that of being multiplied by the same ratio as the input desired signal and also increased due to supplementary (individual) noise added by each active RF block from the receiver chain. Thus, the overall noise factor is continuously degraded from the receiver input to its output (ADC input). This is clearly shown by the Friis formula (1), where G_i represents the block power gain considered in linear units:

$$NF = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \quad (1)$$

As it states, the overall noise factor of several RF cascaded bocks is mainly set by the first block on the receiver chain, therefore the importance of using a low noise amplifier as the first on the RF chain. Hence, this formula refers to the thermal noise generated by the active devices from the receiver chain and not to the noise existent at the RF front-end input. Normally, the LNA is optimized for minimum noise while achieving moderate/high gain and good linearity. However, particular techniques can be implemented in order to compensate the extra noise produced by the input transistor (buffer) of the LNA. This thermal noise is in fact the noise that must be compensated (e.g. $I_n^2(f)$ in Fig. 1) and is truly minimized by these techniques proposed in the literature. Since it is white, having constant power spectral density within the entire spectrum, and at the same frequency as the signal, its rejection is not possible by filtering. This is the reason why, the LNA structure becomes more complicated, supplementary transistors being added and additional signal paths are created in order to compensate the internal noise at the output. However, the price for a smaller NF is, in this case, a higher power consumption and larger chip area.

III. INPUT BUFFERS FOR LNA

After studying the literature dedicated to CMOS low noise amplifiers, an important conclusion would be that all LNAs use either common source (CS) or common gate (CG) transistors as input stages. This signifies that the noise can be compensated for both CS and CG transistors. However, to do this, two correlated versions of the noise current must be achieved at the circuit input, hence the importance of how the first LNA transistor is configured for simultaneous input impedance matching and noise cancellation.

Regarding the CS stages, it is important to notice that the classical CS amplifier with inductive degeneration, configured in Fig. 2a for wideband matching (narrowband matching without $L_{1,2}$, $C_{1,2}$) and widely used to implement CMOS LNAs in practical transceivers, does not fit the noise cancellation concept. The main reason is the difficulty of obtaining two correlated noise voltages at the gate and drain nodes. This is the reason why, shunt-feedback CS stages are used to implement instant input matching, being suitable for noise compensation. In this regard, three versions are reported in literature: resistive shunt feedback (Fig. 2b) [1-5], resistive shunt feedback with decoupling capacitor (Fig. 2c) [6-9] and shunt feedback CS stage with current reuse (Fig. 2d) [10-17]. The feedback resistor R_f can be replaced by an NMOS transistor (Fig. 2e) [18], too.

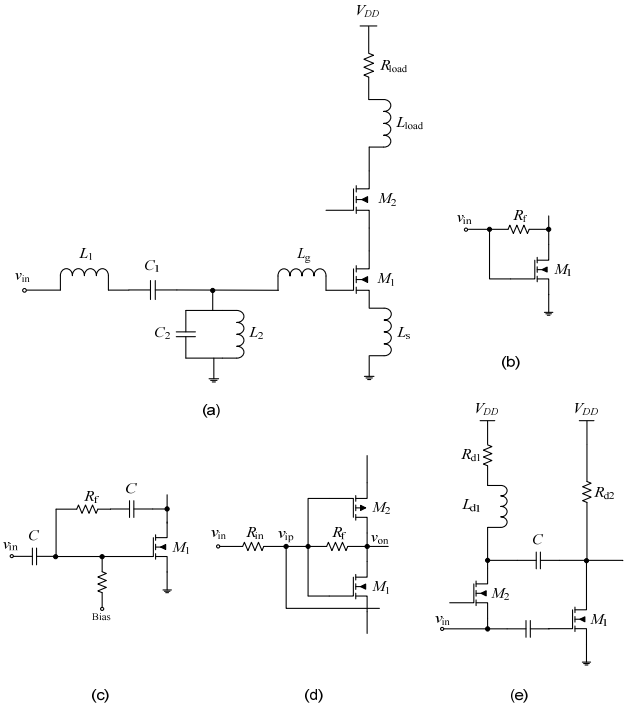

Figure 2. Input stages for CS LNA.

The input buffer shown in Fig. 2b offers very good wideband impedance matching but low NF and power consumption can be hardly achieved across a large frequency range. However, as can be noticed in Fig. 3, this stage has an interesting property from the noise perspective. Thus, thanks to the feedback resistance, the noise current generated by M_1 flows towards the input ground through R_f and R_S (the generator internal resistance, 50Ω). Therefore, it generates two correlated noise voltages $v_{n,Y}$ and $v_{n,X}$ that are in phase while the input and output signals v_X and v_Y have opposite signs. In conclusion, such amplifier allows the noise cancelling implementation, being suitable for single-ended output LNA. However, since $v_{n,Y}$ and $v_{n,X}$ have different amplitude, depending on the R_F/R_S ratio ($A=R_F/R_S=v_{n,Y}/v_{n,X}$), the circuit must be carefully designed in order to truly compensate the noise. For practical implementation, the feedback resistor R_F is larger than R_S, so that its noise can be neglected compared with the main noise contributor M_1. However, a trade-off between impedance matching and noise must be taken into account since R_f degrades NF by approximately 1.2 dB [19].

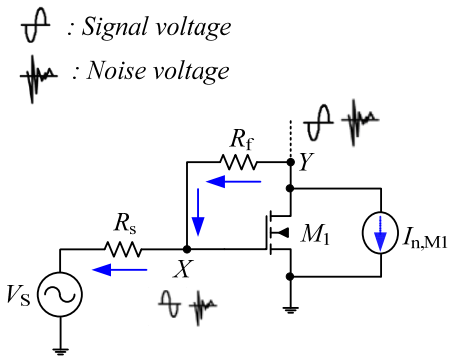

Figure 3. Resistive shunt feedback LNA.

The previous discussion is also available for the input buffer shown in Fig. 2c, the DC decoupling of the feedback resistor -proposed in [19]- being the single difference between these two buffers. Regarding these two architectures, it is not mandatory to connect the feedback resistor at the input buffer drain as it can be connected also to the cascode transistor drain [3, 6, 8, 9].

The third solution is to use a shunt feedback CS stage with current reuse (Fig. 2d). The idea behind this topology is that the same transconductance g_m can be achieved with less current (power consumption) by replacing the single NMOS CS amplifier (M_1) with two transistors (M_{11} and M_{12}), as illustrated in Fig. 4. Well-known as the classical inverter topology, this was also proposed as amplifier [20]. In this case, the equivalent transconductance is the sum of both transconductances. Since achieving low noise figure imposes large transconductance for CS amplifiers, using an inverter topology offers the same noise figure with half power consumption. The supplementary resistor R_f helps for adjusting the error of the noise figure compensation. In addition, such circuit can easily be matched at the input since $Z_{in}=1/(gm_1+g_{m2})$. From the noise perspective, the discussion is the same as above, with the remark that two noise currents are compensated ($I_{n1}^2(f), I_{n2}^2(f)$) in this case. Moreover, the signal voltage has opposite sign at the inverter output while the noise has the same phase at both input and output, therefore the transistor noise can be cancelled.

As can be noticed from the previous architectures, an important advantage of the CS amplifiers over the classical

inductively degenerated CS LNA consists in occupying less chip area, on-chip inductors not being required. However, blocking capacitors still increase the total area.

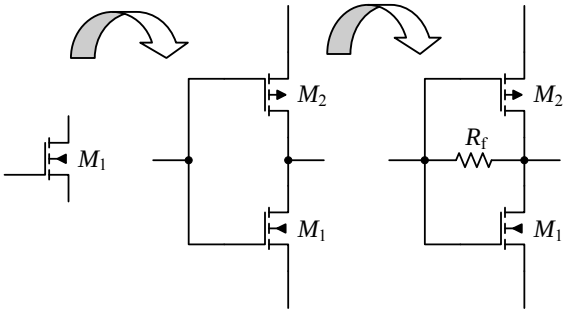

Figure 4. Principle of current reuse.

CG topology is widely used in literature to implement noise compensated LNAs, this stage offering two advantages over the CS counterpart:

1. It can be simply matched at the input by adjusting the biasing current, therefore no supplementary (passive) component being required. In addition, it already offers wideband matching while the CS stage must use supplementary shunt-feedback to achieve the same frequency performances.

2. As shown in Fig. 5, the CG case is similar to the CS one from the noise perspective. Thus, its channel noise can be modeled in the same way, with a noise current source inserted between drain and source and having the same polarity. As can be noticed, two correlated versions of the current noise source and with opposite phases are naturally available for further signal treatment in this case. Therefore, even though having larger noise than the CS counterpart, this stage is more attractive when implementing noise cancellation schemes, more simplified in this case.

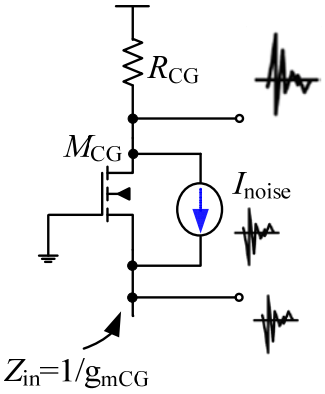

Figure 5. CG noise source.

As in the CS case, there are several topology variations proposed in the literature, depending on the impedance used to ground the transistor source terminal. In this regard, grounding the CG transistor source with current sources [21], resistors [22-24], (choke) inductors [25-41], transistors [42-49] and even (auto) transformers [50-55] were proposed in the literature (Fig. 5). All these architectures are implemented, as in the CS case, with noise cancellation.

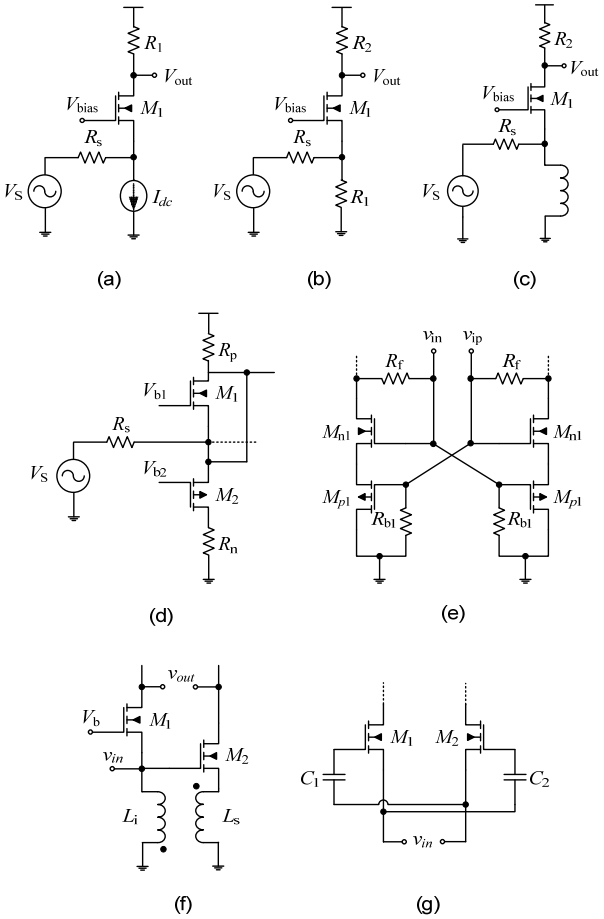

Figure 6. CG topologies with (a) current sources, (b) resistors, (c) inductors, (d-e) transistors, (f) transformers for single-ended and (f) cross-coupled transistors for differential input.

IV. The Principle of Noise Cancelling

With the two input buffers reviewed above, it is interesting to find out how the internal thermal noise can be compensated for a CS amplifier and CG respectively. However, before doing this, it is worth reviewing several things:

a) The scope of implementing the noise cancellation technique is to increase the signal-to-noise ratio at the circuit output (SNR_{out}). Although the circuit is noisier at the input, it offers a better SNR with noise compensation. In this regard, all references mentioned in this article (and resumed below) report sufficiently low NF, even in cases where NF might seem high, such as NF ~ 3...4 dB, as in the case of (ultra) wideband amplifiers.

b) In addition to the advantages presented above, the noise cancellation scheme decouples the matching problem and noise optimization, the trade-off between noise and impedance matching being avoided. This constitutes a real benefit for practical LNA design.

c) The main idea behind the noise cancelling concept is to achieve two correlated versions of the LNA input stage (CS or CG) noise signal and adding them at the circuit output without affecting the input signal. In this way, the input signal is amplified at the output (since there are two signal paths) while the noise is minimized. Noise studying can be done either working with currents or voltages. Since all RF circuits operate with voltages and not currents, all authors prefer to present their technique using voltages, fact that makes the study easier and more intuitive. This review presents the noise problem from the same voltage perspective, as already shown in Fig. 3 and 5.

The noise compensation problem can be split in two parts: achieving, no matter how, two correlated versions of the input noise and adding them at the output, respectively. As the cancellation principle works, it seems that the input buffer (and how the correlated noises are obtained) and the adder scheme are dependent on each other. Therefore, an important remark here is that a particular adder is typical for some input schemes while a particular input scheme suits best a particular adder. As can be notice when studying the noise cancellation schemes proposed in the literature, single-ended and differential output LNAs signify two different adders. A first step into choosing or designing a particular compensation is to decide what adder topology is to be used and preferable. These adders are shown in Fig.7.

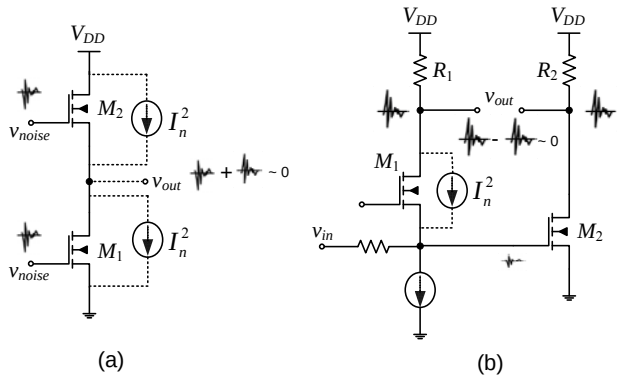

Figure 7. Adders for noise cancelling principle, single-ended (a) and differential (b).

As can be noticed, single-ended adding topology is used when having two in-phase correlated versions of the input noise voltage, while differential one is suitable for the case with opposite phases. Table I classifies the LNAs depending on the single-ended/differential topology.

TABLE I. LNAS CLASSIFICATION

Input	**Output**			
	CS input stage		*CG input stage*	
	SE	*DIFF*	*SE*	*DIFF*
Single-ended (SE)	1-3, 5,6,8-12, 15,17,18	16	23, 25,26, 32,38,40-42,44-46, 48,49,52-54	21,22,24, 30,31,34, 36,37,50, 55
Differential (DIFF)	-	4,7,13, 14	-	27-29, 33,35,39, 43,47,51

In the table above, the single-ended to differential amplifiers are known also as active baluns. In the same time, several output differential topologies use external passive baluns in order to deliver single-ended outputs [22, 34, 50], easier to measure. In the meantime, transformers type baluns can be used to apply differential signals from a single-ended input source, with the main advantage of biasing the LNA [51]. However, these baluns are required for measurement only since a (differential) mixer usually follow the LNA (if SAW filter not required after the LNA), therefore the circuit still remains differential, being considered in Table 1 as fully differential. Therefore, the fact that a circuit is reported in literature as differential does not necessary mean that the noise cancellation principle can be implemented in or requires differential topology. The cross-coupled technique shown in Fig. 6g clearly envisages differential topologies.

Other two remarks can be mentioned here:

1. The noise cancelling technique is not affected by and does not depend on the circuit output resistance, which is an important advantage.

2. There is no 'pure' CG based LNA, all LNAs using CG buffers at the input makes use of a second CS transistor to further process the second correlated noise version, even the cross-coupled one. Such amplifiers are in fact CS-CG LNAs, such as the baluns (SE input - DIFF output) in Table I.

3. The advantage of single-ended topology (Fig. 7a) over the differential one consists in offering instantaneous impedance matching at the output, since the output load 'sees' the source of M_2 (NMOS transistor) which can offer an output impedance of $1/g_{m2}=50\Omega$.

Putting together the buffers shown in Fig. 2, Fig 6 and the output stages shown in Fig. 7, the principle of noise cancelling can be generalized as shown in Fig. 8, each reference coming with little changes on how the signal path is implemented, how many stages has the amplifier (several stages automatically means increased gain), how signal distortions are minimized, and so on.

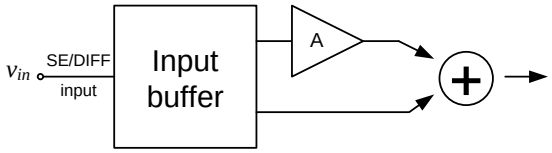

Figure 8. Noise cancellation principle; the amplifier is usually a CS stage.

The smallest noise figures achieved thanks to the noise cancellation principle are 0.45 dB (for in-phase component, thanks to the technique called 'noise squeezing') [40], 1.4-1.7 dB [4] and 1.9 dB [20]. The second LNA is a fully differential broadband CS topology, implemented in a 90nm CMOS process and using the architecture shown in Fig. 6e. It achieves a high gain of 20 dB and a good IIP3 of -1.5 dB. The third is a wideband LNA, it achieves an NF of 1.9 dB while offering a gain of 19.8 dB in a wide bandwidth (0.2-6.6 GHz). Its IIP3 is 1.6 dB, the circuit being implemented in a 0.13µm CMOS process. In the meantime, the largest gains achieved by the LNAs designed with noise cancelling are reported in two references proposing RF front-ends (LNA+mixer). The maximum overall gains are 36 dB [17] and 26-28 dB [31], the first being a 0.2-2 GHz DRM/DAB/DVB-H receiver while the

second one a 3.1-10.6 GHz UWB receiver (with flat gain and NF). They report a noise figure of 3.1-6.1 dB [17] and 4.8-6.2 dB [31], while being implemented in 0.18 μm and 0.13 μm CMOS process, respectively. As it can be noticed, it is still difficult to reach large gains and very low noise factors. In any case, the smaller noise factor, large gain and easier impedance matching make the noise cancelling an attractive technique for implementing the future LNAs on the market.

V. CONCLUSIONS

The principle of thermal noise cancellation, as applied for CMOS low noise amplifiers, was discussed in this article. Based on an exhaustive and up-to-date literature, the article offers a review of this principle from a systematic point of view while trying to remain as general as possible. The most important conclusion that can be drawn from this review is that the thermal noise cancelling imposed itself, thanks to the good results reported in the literature and its simplicity, as a viable solution for implementing very low noise figure CMOS amplifiers. Beside distortion cancelling, already proposed in literature, this principle clearly changed the LNA history.

REFERENCES

[1] Qiang Li; Y.P. Zhang; J.S. Chang, "An Inductorless Low-Noise Amplifier with Noise Cancellation for UWB Receiver Front-End", IEEE Asian Solid-State Circuits Conference (ASSCC), pp. 267-270, 2006

[2] Qiang Li; Y.P. Zhang, "A 1.5-V 2–9.6-GHz Inductorless Low-Noise Amplifier in 0.13-μm CMOS", IEEE Transactions on Microwave Theory and Techniques, vol. 55, no. 10, pp. 2015-2023, 2007

[3] Xiao Wang; W. Aichholzer; J. Sturm, "A 0.1–4GHz resistive feedback LNA with feedforward noise and distortion cancelation", Proceeding of the ESSCIRC, pp. 406 - 409, 2010

[4] M. El-Nozahi; A.A. Helmy; E. Sánchez-Sinencio; K. Entesari, "An Inductor-Less Noise-Cancelling Broadband Low Noise Amplifier With Composite Transistor Pair in 90 nm CMOS Technology", IEEE Journal of Solid-State Circuits, vol. 46, no. 5, pp. 1111 - 1122, 2011

[5] Ke-Hou Chen; Shen-Iuan Liu, "Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 2, pp. 305 - 314, 2011

[6] Shih-Chih Chen et al., "The design of full-band (3.1–10.6GHZ) CMOS UWB low noise amplifier with thermal noise canceling", Asia-Pacific Microwave Conference (APMC), pp. 409 - 412, 2006

[7] Xi Chen; J. Silva-Martinez; S. Hoyos, "A CMOS differential noise cancelling low noise transconductance amplifier", IEEE Circuits and Systems Workshop: System-on-Chip - Design, Applications, Integration, and Software, pp. 1 - 4, 2008

[8] Jianyun Hu; Yunliang Zhu; Hui Wu, "An Ultra-Wideband Resistive-Feedback Low-Noise Amplifier with Noise Cancellation in 0.18μm Digital CMOS", IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 218 - 221, 2008

[9] Hyewon Kim et al., "A 12mW 5GHz wideband low-noise amplifier in 0.13μm CMOS using noise cancellation", IEEE MTT-S International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals (IMWS-IRFPT), pp. 1 - 2, 2011

[10] F. Bruccoleri; E. A. M. Klumperink; B. Nauta, "Noise canceling in wideband CMOS LNAs", IEEE International Solid-State Circuits Conference (ISSCC), vol. XLV, pp. 406 - 407, 2002

[11] F. Bruccoleri; E. A. M. Klumperink; B. Nauta, "Wide Band CMOS Low-Noise Amplifier Exploiting Noise Cancellation", Workshop on Circuits, Systems and Signal Processing (ProRISC), 2002

[12] F. Bruccoleri; E. A. M. Klumperink; B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling", IEEE Journal of Solid-State Circuits (JSSC), vol 39, no. 2, pp. 275-282, 2004

[13] Wang Keping; Wang Zhigong, "A Broadband Noise-Canceling CMOS Differential LNA for 50-860MHz TV Tuner", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 413 - 416, 2007

[14] Wang Keping; Wang Zhigong, "A Broadband Noise-Canceling CMOS Differential LNA for 50-860MHz TV Tuner", International Conference on Microwave and Millimeter Wave Technology (ICMMT), Vol 2, pp. 835 - 838, 2008

[15] K.S. Chen; N.T. Hsu; K.C. Lu; T.S. Horng; J.M. Wu, "A variable gain low-noise amplifier with noise and nonlinearity cancellation for DVB applications", Asia Pacific Microwave Conference (APMC), pp. 1144 - 1147, 2009

[16] Custódio, J.R. et al., "A small-area self-biased wideband CMOS balun LNA with noise cancelling and gain enhancement", NORCHIP, pp. 1 - 4, 2010

[17] Wang Keping, Wang Zhigong; Lei Xuemei, "Noise-canceling and IP3 improved CMOS RF front-end for DRM/DAB/DVB-H applications", Journal of Semiconductors, vol. 31, no. 2, pp. 025006-1 - 025006-5, 2010

[18] J.M. Wu; N.K. Yang; S.C. Li, "A low power WiMAX LNA with noise cancellation", International Conference on Communications and Networking in China (ChinaCOM), pp. 286 - 288, 2008

[19] Hsien-Ku Chen; Da-Chiang Chang; Ying-Zong Juang; Shey-Shi Lu, "A Compact Wideband CMOS Low-Noise Amplifier Using Shunt Resistive-Feedback and Series Inductive-Peaking Techniques", IEEE Microwave and Wireless Components Letters, vol. 17, no. 8, pp. 616 - 618, 2007

[20] A. N. Karanicolas, "A 2.7V 900MHz CMOS LNA and Mixer", IEEE Journal of Solid-State Circuits (JSSC), vol 31, no. 12, pp. 1939 - 1944, 1996

[21] I. Bastos; L.B. Oliveira; J. Goes; M. Silva, "MOSFET-only wideband LNA with noise cancelling and gain optimization", International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 306 - 311, 2010

[22] S.C. Blaakmeer; E.A.M. Klumperink; D.M.W. Leenaerts; B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling", IEEE Journal of Solid-State Circuits (JSSC), vol 43, no. 6, pp. 1341 - 1350, 2008

[23] Mingkun Gao; Yi Wang; Yunfeng Wang; Donghui Guo, "Design of wideband CMOS LNA with active inductor and using noise-canceling technique", International Conference on Anti-counterfeiting, Security, and Identification in Communication (ICASID), pp. 262 - 265, 2009

[24] Hongrui Wang; Li Zhang; Zhiping Yu, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 8, pp. 1993 - 2005, 2010

[25] Chih-Fan Liao; Shen-Iuan Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receiver", IEEE Custom Integrated Circuits Conference (CICC), pp. 161 - 164, 2005

[26] S.M.R. Hasan; Jie Li, "A Bias-Controlled Noise-Canceling CMOS Tuned Low Noise Amplifier for UWB Transceivers", IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 1205 - 1208, 2007

[27] Dong-Gu Im; Seong-Sik Song; Hong-Teuk Kim; Kwyro Lee, "A Wide-Band CMOS Variable-Gain Low Noise Amplifier for Multi-Standard Terrestrial and Cable TV Tuner", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 621 - 624, 2007

[28] H. Ali; K. Sharaf, "Noise cancellation techniques in multi-standard low noise amplifiers", Internatonal Conference on Microelectronics, pp. 227 - 230, 2007

[29] J. Jussila; P. Sivonen, "A 1.2-V Highly Linear Balanced Noise-Cancelling LNA in 0.13-μm CMOS", IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 579 - 587, 2008

[30] Manstretta, D., "A broadband low-noise single-ended input differential output amplifier with IM2 cancelling", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 79 - 82, 2008

[31] Bo Shi; Michael; Yan Wah Chia, “Design of a 3.1–10.6 GHz noise-canceling CMOS UWB receiver front-end”, Asia-Pacific Microwave Conference (APMC), pp. 1 - 4, 2008

[32] A. Mirvakili; M. Yavari, “A noise-canceling CMOS LNA design for the upper band of UWB DS-CDMA receivers”, IEEE International Symposium on Circuits and Systems (ISCAS), pp. 217 - 220, 2008

[33] Jinhua Liu; Guican Chen; Ruizhi Zhang, “Design of a noise-canceling differential CMOS LNA for 3.1–10.6 GHz UWB receivers”, IEEE International Conference on ASIC (ASICON), pp. 1169 - 1172, 2009

[34] Thu Nga Tran Thi; Chirn Chye Boon; Manh Anh Do; Kiat Seng Yeo, “Reciprocal noise canceling low power UWB LNA”, International SoC Design Conference (ISOCC), pp. 13 - 16, 2009

[35] Donggu Im; Ilku Nam; Kwyro Lee, “A Low Power Broadband Differential Low Noise Amplifier Employing Noise and IM3 Distortion Cancellation for Mobile Broadcast Receivers”, IEEE Microwave and Wireless Components Letters, vol. 20, no. 10, pp. 566 - 568, 2010

[36] D. Navaratne; A. Beaulieu; L. Belostotski, “Noise figure optimization of a noise-cancelling wide-band CMOS LNA”, IEEE International NEWCAS Conference (NEWCAS), pp. 125 - 128, 2010

[37] Lan You, Chuan Wang, Falin Liu, “A 3-5 GHz Ultra-wideband Low Noise Amplifier Employing Noise Cancellation”, IEEE International Conference on Ultra-Wideband (ICUWB), vol. 1, pp. 1 - 4, 2010

[38] R. Mirzalou; A. Nabavi; G. Darvish, “A highly linear LNA with noise cancellation for 5.8–10.6 GHz UWB receivers”, Iranian Conference on Electrical Engineering (ICEE), pp. 1 - 6, 2011

[39] A.R. Ximenes; J.W. Swart, “A wideband noise canceling low-noise amplifier for 50MHz–5GHz wireless receivers in CMOS technology”, IEEE International New Circuits and Systems Conference (NEWCAS), pp. 197 - 200, 2011

[40] Wooram Lee; E. Afshari, “An 8GHz, 0.45dB NF CMOS LNA employing noise squeezing”, IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 1 - 4, 2011

[41] P. Bindu; P.C. Subramaniam, “CMOS wide band Low Noise Amplifier with current reuse and noise cancellation”, International Conference on Communications and Signal Processing (ICCSP), pp. 65 - 69, 2011

[42] S. Chehrazi; A. Mirzaei; R. Bagheri; A.A. Abidi, “A 6.5 GHz wideband CMOS low noise amplifier for multi-band use”, IEEE Custom Integrated Circuits Conference (CICC), pp. 801 - 804, 2005

[43] A. Amer; E. Hegazi; H.F. Ragaie, “A 90-nm Wideband Merged CMOS LNA and Mixer Exploiting Noise Cancellation”, IEEE Journal of Solid-State Circuits, vol. 42, no. 2, pp. 323 - 328, 2007

[44] Wei-Hung Chen; Gang Liu; B. Zdravko; A.M. Niknejad, “A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation”, IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 61 - 64, 2007

[45] Wei-Hung Chen; Gang Liu; B. Zdravko; A.M. Niknejad, “A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation”, IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1164 - 1176, 2008

[46] Donggu Im; Ilku Nam; Hong-Teuk Kim; Kwyro Lee, “A Wideband CMOS Low Noise Amplifier Employing Noise and IM2 Distortion Cancellation for a Digital TV Tuner”, IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 686 - 698, 2009

[47] Yuh-Shyan Hwang, San-Fu Wang, Jiann-Jong Chen, “A differential multi-band CMOS low noise amplifier with noise cancellation and interference rejection”, International Journal of Electronics and Communications (AEU), vol. 64, no. 10, pp. 897 - 903, 2010

[48] Yuh-Shyan Hwang; San-Fu Wang; Shou-Chung Yan; Jiann-Jong Chen, “An inductorless wideband noise-cancelling CMOS low noise amplifier with variable-gain technique for DTV tuner application”, International Journal of Electronics and Communications (AEU), vol. 64, no. 11, pp. 1009 - 1014, 2010

[49] F. Ghadimipoor; H.G. Garakani, “A noise-canceling CMOS low-noise Amplifier for WiMAX”, International Conference on Electronic Devices, Systems and Applications (ICEDSA), pp. 165 - 169, 2011

[50] S.C. Blaakmeer; E.A.M. Klumperink; D.M.W. Leenaerts; Bram Nauta, “A wideband noise-canceling CMOS LNA exploiting a transformer”, IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 137 - 140, 2006

[51] Youchun Liao; Zhangwen Tang; Hao Min, “A CMOS wide-band low-noise amplifier with balun-based noise-canceling technique”, IEEE Asian Solid-State Circuits Conference (ASSCC), pp. 91 - 94, 2007

[52] T. Kihara; T. Matsuoka; K. Taniguchi, “A 1.0 V, 2.5 mW, transformer noise-canceling UWB CMOS LNA”, IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 493 - 496, 2008

[53] Feng Lu; Lei Xia, “A CMOS LNA with Noise Cancellation for 3.1-10.6 GHz UWB Receivers Using Current-Reuse Configuration”, IEEE International Conference on Circuits and Systems for Communications (ICCSC), pp. 824 - 827, 2008

[54] M. Forouzanfar; S. Naseh, “High gain CMOS UWB LNA employing thermal noise cancellation”, IEEE International Conference on Ultra-Wideband (ICUWB), pp. 118 - 122, 2009

[55] Ming-Yeh Hsu; Chao-Shiun Wang; Chorng-Kuang Wang, “A low power high reliability dual-path noise-cancelling LNA for WSN applications”, IEEE Custom Integrated Circuits Conference (CICC), pp. 1 - 4, 2010