Approaches in Implementing Multi-band CMOS Low Noise Amplifiers

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Abstract—**This paper reviews the major contributions proposed in literature for implementing multi-band low noise amplifiers in CMOS technology. Concurrent, switched and switched concurrent low noise amplifiers are investigated. Advantages and drawbacks are also discussed. The article tries to offer good insights on the implementation of multi-band low noise amplifiers.**

Keywords-CMOS; low noise amplifier; multi-band; noise figure

I. INTRODUCTION

The increasing number of wireless standards which a mobile terminal must cover pushes more and more pressure on the RF Front-end and LNA in particular. Being the first active functional block on the RF path, the LNA must be able to increase the input signal power with the smallest noise as possible. Many design methodologies were proposed in the literature in order to fulfill the novel constraints in terms of chip area, power consumption and spectrum efficiency. Currently, the mobile terminals existent on the market use a bank of single band LNAs in order to cover multiple bands, as shown in Fig. 1 [1].

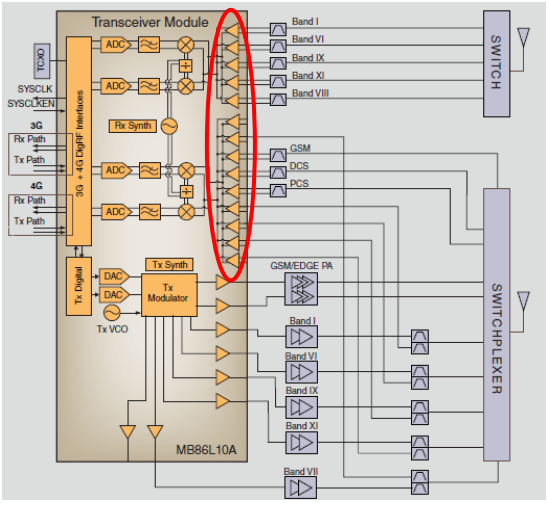

Figure 1. Fujitsu MB86L10A 2G/3G/LTE multimode multi-band transceiver.

Such LNAs are narrow-band amplifiers, designed for a single frequency band/particular telecommunication standard and usually implemented with CS (common source) stages. One amplifier only is selected according to the instantaneous operational band, hence the equivalent name of *switched LNAs*. If wideband applications are envisaged (such as UWB), several narrow-band LNAs can be cascaded, a wideband amplifier being obtained in this case [2, 3]. However, this does not necessarily mean that the MOS transistor is limited to narrow-band applications. In fact, the transistor transconductance is inherently wideband, usually passive resonant circuits being used to shape its frequency response, such stage being able to provide gain and matching at other frequencies with no penalty from the perspective of power consumption.

The multi-band LNAs can be classified into three classes: concurrent LNAs (dual and triple band), switched LNAs (dual, triple and quad-band) and switched concurrent or pseudo-concurrent LNAs (dual and quad-band). Concurrent LNAs are amplifiers capable of simultaneous operation (with narrow-band gain and matching) at several frequency bands, usually two or three (as proposed in the literature), while maintaining minimum low noise figure and high linearity. Using such amplifiers imposes some major changes of the receiver architecture such as using multi-band antennas and RF SAW filters respectively. Although the frequency planning must be changed too, it is obvious that the receiver gains in terms of chip area (higher integration) and power consumption (by current reuse structure) when using multi-band LNA.

Any multi-band LNA, concurrent or switched amplifier, can be split into three stages: the amplifier, input and output matching networks/stages. Each stage is discussed in the followings sections. As it will be noticed, passive networks are used to match all multi-band amplifiers at the input and output.

II. THE AMPLIFIER

The common source stage (CS) is mostly used to implement single band LNAs since it offers minimum noise figure. In addition, cascode stages may be used to provide wideband transconductance, high gain, good reverse isolation (hence good stability) and low noise figure. Dual- and triple-band LNAs are no exception, all architectures proposed in the literature making use of the cascode stage with inductive degeneration (Fig. 2a). The source inductor allows for easier biasing and narrowband input impedance matching, with the price of larger chip area (L_s implemented on-chip) and smaller gain ($g_m=1/2\omega_0 L_s$ at the resonant frequency). This is the reason why L_s is chosen as small as possible, even much smaller than the supplementary gate inductance. A single-band

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CS LNA is simply matched by adding a supplementary gate inductance L_g as matching network (MN), narrow impedance matching being implemented at the frequency of interest in this case (Fig. 2b). The input impedance has a form as expressed by (1), the real part being tuned to 50Ω at the frequency of interest (of resonance). L_g is implemented on-chip, in some cases a bonding wire being used instead.

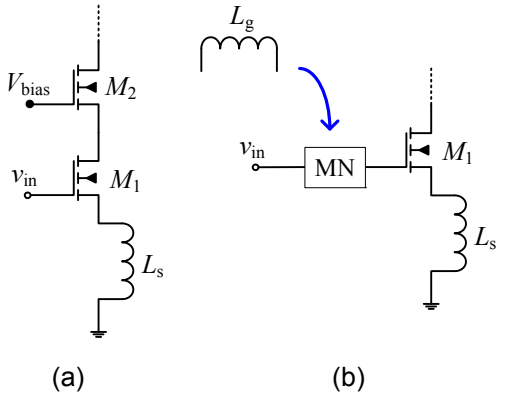

Figure 2. Cascode stage with inductive degeneration.

$$Z_{in}(s) = s(L_g + L_S) + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}} \qquad (1)$$

Related to the amplifier stage, two methods can be used to design switched multi-band LNAs, either implementing two or more identical stages (covering different frequencies) on the same chip, each one being selected according to the frequency plan, or implementing the input CS transistor M_1 as two or more transistor with different sizes and connected in parallel, so that only one is chosen according to the frequency plan.

III. Input Matching Network

A. Concurrent LNAs

In order to work at two or three distinct frequencies, the LNA must be firstly matched at the frequencies of interest. If a single band LNA is simply matched by inserting a gate inductance, as discussed above, simultaneous matching a LNA at two frequencies of interest is not so simple. Yet, different techniques were proposed during the last decade to overcome this problem. To understand these artifices related in fact to the passive networks only, it is sufficient to start with Z_{in}, as expressed by (1). Thus, being equivalent to a real series LC network (due to the resistive part), this matching network behaves as a 'short-circuit' around the frequency of interest, letting the frequencies of interest to pass to the LNA while attenuating other frequencies. In fact, this is also the essence of this (basic and widely used) impedance matching technique.

The multi-band matching techniques envisage the manipulation of the LNA transfer function or MN impedance in such manner that supplementary transmission zeros are inserted. The basic dual-band matching network consists of a parallel LC network in series with L_g (a LLC MN), as shown in Fig. 3a [4, 5]. Originally proposed for 2.45/5.25 GHz bands, this technique was also used to implement multi-band LNAs designed for other frequency pairs such as 1.8/5.8 GHz [6], 0.9/2.14 GHz [7], 0.9/2.4 GHz [8], 2.4/5.2 GHz [9, 10] and 2.6/5.2 GHz [11]. Since the parallel LC network is 'open' at its resonant frequency, it inserts a pole into the transfer function, splitting the single-band matching into dual-band input matching. The LLC network together with transistor input impedance constitutes a 'shunt' and 'open' in series, which can be set in such manner that the circuit is dual-band matched. Z_{in} has in this case the following value:

$$Z_{in}(s) = s(L_g + L_S) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_S}{C_{gs}} + \frac{sL_1}{1 - s^2 L_1 C_1} \qquad (2)$$

Since the imaginary part has two possible solutions when zeroed, therefore $Z_{in}(s)$ being real at these two frequencies, the amplifier is fully matched, being dual-band. Thus, the parallel LC network resonates with C_{gs} and L_s at two frequencies set by all four parameters (e.g. $\omega_1 = f(L_g, C_{gs}, L_1, C_1)$ and $\omega_2 = f(L_g, C_{gs}, L_1, C_1)$). It is obvious that by changing different parameters, such as L_g, L_1 and C_{gs} (inserting a supplementary capacitor between gate and source as proposed in [10, 11]), a large number of multi-band LNA topologies covering different frequency pairs can be generated.

Another type of LLC MN reported in [12] is shown in Fig. 3b. Such LLC network tunes out the gate capacitance at two frequencies, 2.45/5.25 GHz in this case. A more complex narrowband LC matching structure, easier to design, has been reported in [13] for the frequency bands 0.9/1.8 GHz.

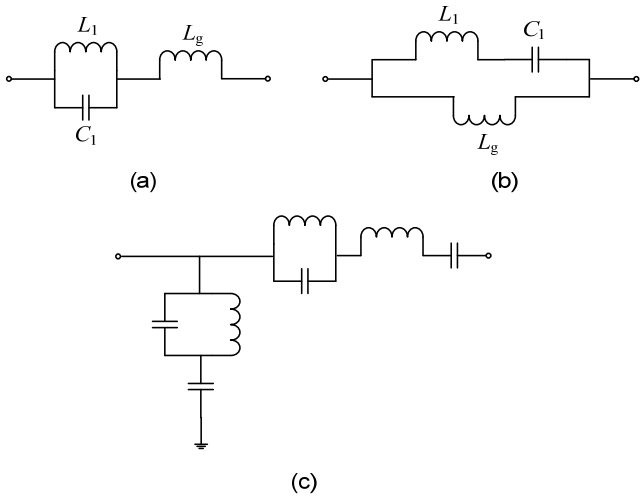

Figure 3. Narrowband MN for dual-band LNAs.

The structures reported above provide narrowband matching. However, wideband matching networks were also reported in literature. The simplest structure suitable for CS LNAs consists of a single parallel LC resonator inserted at the amplifier input as shown in Fig. 4a [14], the amplifier covering the 0.9/1.8 GHz bands. The same MN was also used to implement a triple-band LNA covering the 2.6/3.6/5.5 GHz [15]. In this case, the bandwidth of interest is selected by the output resonators. Two more complicated networks used to implement a triple-band LNA covering the 1.8/2.45/5.25 GHz [16] and 2.4/3.5/5.2 GHz [17] are shown in Fig. 4b and Fig. 4c respectively.

Transformers can be also used to implement multi-band matching but in other technologies, such as GaAs [18] and SiGe [19].

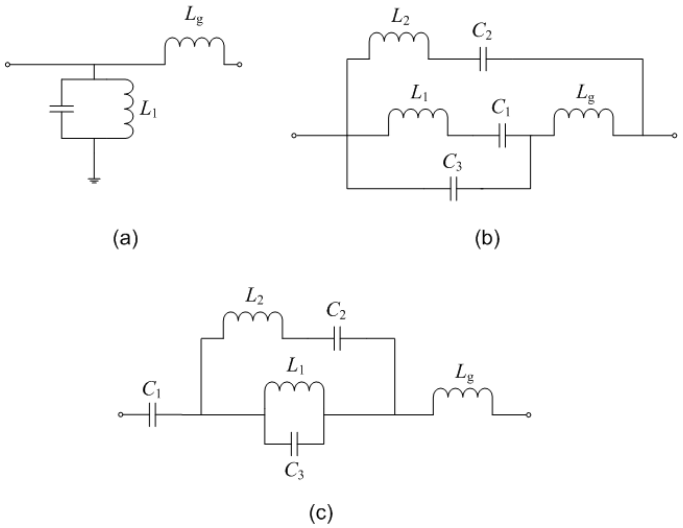

Figure 4. MN for triple-band LNAs.

B. Switched LNAs

Such amplifiers have the capability of tuning their frequency band mainly by changing the value of passive elements (capacitances - Fig. 5a or inductances - Fig. 5b), by means of a PMOS/NMOS active switch. As proposed in literature, these amplifiers usually cover two, three or even four distinct frequency bands. Owing to their low r_{on} and larger gain, NMOS transistors functioning at the linear region are preferred. As it can be seen in Fig. 1, RF switches are widely used in RF Front-ends. However, using active switches together with LNAs comes with several drawbacks such as nonlinearity, noise and parasitic resistance.

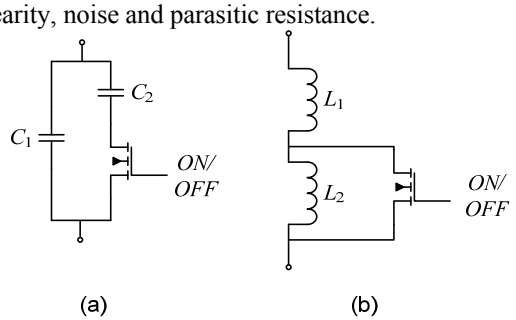

Figure 5. Variable capacitor (a) and inductance (b).

The variable capacitor shown in Fig. 5a can be used to change the gate to source capacitance value C_{gs}, by inserting this network between transistor gate and source, as reported in [20]. The LNA covers in this case the EDGE/Bluetooth bands. The same tuning scheme has been used to implement LNAs covering the bands 1.8/2.14 GHz (CDMA/WCDMA) [21] and 1.8/2.4 GHz [22, 23]. Tuning inductors (Fig. 5b) was proposed for changing L_g value in case of a quad band LNA covering the 1.9/2.4/3.5/5.2 GHz (GSM/LTE/WiMAX/WLAN) bands [24].

There is also the possibility of simultaneous tuning of L_g and C_{gs}, both switches shown above being used. This is the case of several dual-band LNAs proposed in literature, covering the bands 2.4/5.2 GHz [25, 26] and 0.9/1.95 GHz [27], and even triple-band LNA covering 0.9/2.4/5.2 GHz [28].

C. Pseudo-concurrent LNAs

Pseudo-concurrent LNAs are concurrent amplifiers which, when set, are able to cover either a set of frequencies (two or three) or another set of frequencies (two or three). The key element of such LNA is the input matching network that must provide concurrent match for at least 3 frequencies. Such example of matching network was reported in [29], providing matching at 4 frequencies (Fig. 6a). Another matching network implemented with two L_g switched inductors and two C_{gs} switched capacitors was used in [30] to implement a quad-band concurrent LNA, covering the bands 0.9/1.8 GHz and 0.9/2.4 GHz respectively. An interesting MN (Fig. 6b) was used in [31] to design a switchable single/double band LNA (3.5 GHz && 2.4/5.2 GHz). In this case, L_1-C_1 implement a low-pass filter and L_2-C_{gs} a high-pass filter, all together being a bandpass filter. The band of 3.5 GHz is covered by inserting a switched capacitor C_2 that cuts the higher frequencies, since it has a lower impedance than the bandpass filter at higher frequencies.

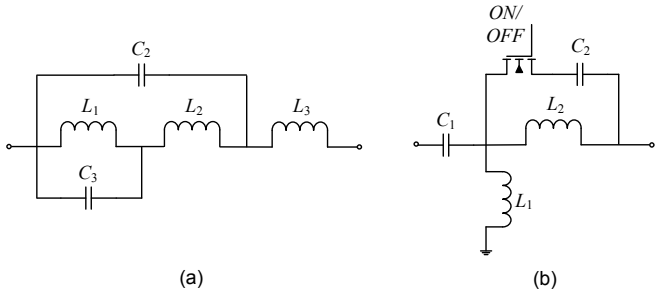

Figure 6. MN for quad-band concurrent LNA (a) and MN for single/double band LNA (b).

D. Multi-band LNA with continuous tuning

An innovative method of implementing a tuned multi-band CS LNA consists in tuning the gate inductance L_g. Studying (1), it is obvious that L_s sets the resonant frequency while L_s and C_{gs} set the real part of Z_{in}. This signifies that changing L_g will tune the LNA band only, fact exploited in [32], where a floating active inductor is used to implement L_g (Fig. 7). RFC is an external shock inductor and C_c is a decoupling capacitor. The amplifier has a tuning range of 1.9-2.4 GHz, careful design must be applied since the active inductor inserts supplementary noise.

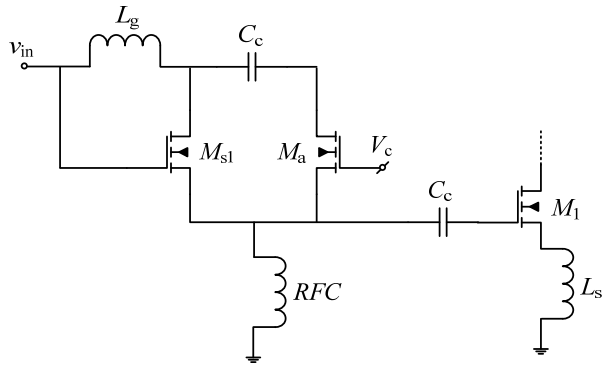

Figure 7. MN with active floating inductor.

IV. Output Stages

Even though the input and output of a stand-alone LNA must be matched for maximum power transfer, the output of an integrated LNA does not necessarily have to be matched since it usually drives the capacitive input of a down-conversion mixer. This is the reason why, the output stage/load only of a LNA is taken into consideration in this paper. According to theory, a LNA consists of a transconductance stage -used to translate the input voltage to output current- and a load to translate the output current to output voltage. Since the effective voltage gain is dependent on the output impedance value Z_L, different loads can be used for LNAs in order to achieve higher gains, such as resistors, inductors and resonators. RF choke inductors [6, 15, 18, 22, 24-26] are an attractive choice since their impedance increases with frequency while biasing the transistor, thus being a good solution for GHz applications. However, careful design must be applied since large Z_L generates large voltage swing at the transistor drain which can reduce the transistor voltage headroom, therefore moving the static point to linear region when strong signals are applied to the input. In this case, the function of the LNA is compromised. This problem becomes more stringent in the case of LC parallel resonators (Fig. 8a) which offer less headroom than the simple inductors. However, inserting a parallel resistance increases the bandwidth and headroom while decreasing the quality factor and gain. In the same time, series LC resonators have been proposed as alternatives, choke inductors or even parallel LC network still being used for biasing purposes [12]. Contrary to the parallel case, the series resonator generates low drain voltage swing at resonance, most of the AC drain current flowing through the resonator, therefore the Miller effect being completely avoided. Such load favors lower DC biasing voltage, making the LNA suitable for low power applications and improving the transistor linearity with the price of lower gain. The series branch is very useful for multi-band applications, most dual-band architectures using series LC branches at the output.

There are two ways of interconnecting the LC series network, the transfer function being affected differently in each case. The first case consists of inserting the LC resonator between transistor drain and the biasing source (V_{DD}). Since the path is 'short' at resonance, such topology is used to create a zero in the gain transfer function of the LNA, therefore inserting a notch in the gain characteristic. This is very helpful for dual-band LNAs, where the notch frequency is chosen between the frequencies of interest, thus the image rejection being greatly enhanced. The second method is to use a series branch as load while taking the output voltage from the capacitor, as reported in [12] and shown in Fig. 8b. In this case, two series branches are connected to the output, each one allowing the frequency of interest to pass only. This method is attractive since using multiple series branches has no significant effect on the headroom voltage. Even in this case, a choke inductor must be used to bias the LNA. However, as reported in literature [4, 5, 7-11, 13, 16, 23, 29-31], a multi-resonant load consisting of a series LC branch in parallel with a parallel LC resonator is preferably (Fig. 8c). Such pair offers three frequencies at which the imaginary part of Z_L is zero, one at the notch frequency (set by the series branch only) and other two frequencies that can be set as the frequencies of interest and whose value is set by all four passive elements [7, 10]. Thus, the circuit can be matched at the output while achieving multi-band gain characteristic. This topology suits best the concurrent multi-band configurations, a simple inductor load being sufficient for switched amplifiers [25, 26, 29], switched inductors being also used as load [27, 28, 31].

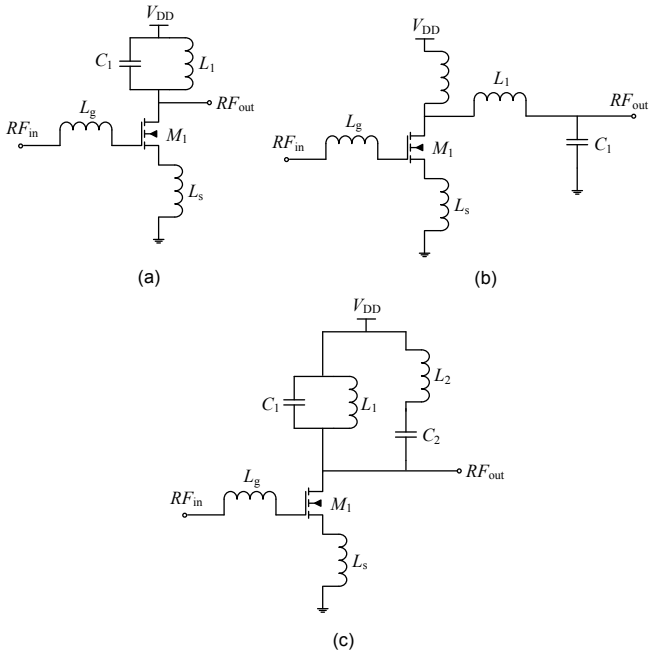

Figure 8. Implementations of LNAs with series and parallel LC resonators.

Conclusions

Three major classes of multi-band low noise amplifiers implemented in CMOS technology were reviewed in this paper. An important conclusion that can be drawn after studying all these topologies is that passive devices constitute a key element for achieving the lowest noise figure, offering in the same time extra freedom degrees for the LNA design and frequency planning scheme. In addition, careful design must be applied to the output stage in order to avoid problems such as nonlinearity and instability, each version offering not only advantages but also drawbacks.

References

[1] http://us.fujitsu.com/micro

[2] C.-P. Chang; C.-C. Yen; H.-Ru Chuang, "A 2.4~6GHz CMOS Broadband High-Gain Differential LNA for UWB and WLAN Receiver", Asian Solid-State Circuits Conference (ASSCC), Vol. 1, pp. 469-472, 2005

[3] Hui-I Wu; R. Hu; C.F. Jou, "Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration", IEEE Microwave and Wireless Components Letters, Vol. 20, No. 7, pp. 402-404, 2010

[4] H. Hashemi; A. Hajimiri, "Concurrent Dual-Band CMOS Low Noise Amplifiers and Receiver Architectures", IEEE Symposium on VLSI Circuits, Vol. 1, pp. 247-250, 2001

[5] H. Hashemi; A. Hajimiri, "Concurrent Multiband Low-Noise Amplifiers—Theory, Design, and Applications", IEEE Transactions on

Microwave Theory and Techniques, Vol. 50, No. 1, Part 2, pp. 288-301, 2002

[6] Mou Shouxian; Ma Jianguo; Yeo Kiat Seng; Do Manh Anh, "An integrated dual-band low noise amplifier for GSM and wireless LAN applications", IEEE Internations System-on-Chip Conference, Vol. 1, pp. 67-70, 2003

[7] M. Ben Amor; A. Fakhfakh; H. Mnif; M. Loulou, "Dual band CMOS LNA design with current reuse topology", International Conference on Design and Test of Integrated Systems in Nanoscale Technology (DTIS), Vol. 1, pp. 57-61, 2006

[8] S. Datta; A. Dutta; T.K. Bhattacharyya, "A gain boosted fully concurrent dual-band interstage matched LNA operating in 900 MHz/2.4 GHz with sub-2dB Noise Figure", IEEE International Conference on Communication Control and Computing Technologies (ICCCCT), Vol. 1, pp. 25-30, 2010

[9] E. Kargaran; B. Madadi, "Design of a novel dual-band concurrent CMOS LNA with current reuse topology", International Conference on Networking and Information Technology (ICNIT), Vol. 1, pp. 386-388, 2010

[10] S. Datta; K. Datta; A. Dutta; T.K. Bhattacharyya, "Fully Concurrent Dual-Band LNA Operating in 900 MHz/2.4 GHz Bands for Multi-standard Wireless Receiver with Sub-2dB Noise Figure", International Conference on Emerging Trends in Engineering and Technology (ICETET), Vol. 1, pp. 731-734, 2010

[11] G. Zhiqiang; L. Dawei; L. Xiaowei; Z. Zhongzhao, "The design of dual-band CMOS low noise amplifier for wireless applications", Academic International Symposium on Optoelectronics and Microelectronics Technology (AISOMT), Vol. 1, pp. 344-347, 2011

[12] S. Hyvonen; K. Bhatia; E. Rosenbaum, "An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply", IEEE Radio Frequency integrated Circuits (RFIC) Symposium (RFIC), Vol. 1, pp. 43-46, 2005

[13] A. Dutta; K. Dasgupta; T.K. Bhattacharyya, "Parasitic-aware robust concurrent dual-band matching network for a packaged LNA", IET Microwaves, Antennas & Propagation, Vol. 3, No. 7, pp. 1094-1101, 2009

[14] M.A. Martins; J.R. Fernandes; M.M. Silva, "Techniques for Dual-Band LNA Design using Cascode Switching and Inductor Magnetic Coupling", IEEE International Symposium on Circuits and Systems (ISCAS), Vol. 1, pp. 1449-1452, 2007

[15] C. Garuda; M. Ismail, "A Multi-band CMOS RF Front-end for 4G WiMAX and WLAN Applications", IEEE International Symposium on Circuits and Systems (ISCAS), Vol. 1, pp. 3049-3052, 2006

[16] C.F. Jou; Kuo-Hua Cheng; Eing-Tsang Lu; Yang Wang, "Design of a fully integrated concurrent triple-band CMOS low noise amplifier", Midwest Symposium on Circuits and Systems, Vol. 3, pp. 1239-1242, 2003

[17] Chih-Yuan Kao; Yueh-Ting Chiang; Jeng-Rern Yang, "A concurrent multi-band low-noise amplifier for WLAN_WiMAX applications", IEEE International Conference on Electro/Information Technology (EIT), pp. 514-517, 2008

[18] G.-L. Ning, Z.-Y. Lei, L.-J. Zhang, R. Zou, and L. Shao, "Design of Concurrent Low-noise Amplifier for Multi-band Applications", Progress in Electromagnetics research C, Vol. 22, pp. 165-178, 2011

[19] Ouail El-Gharniti; E. Kerherve; J.-B. Begueret; D. Belot, "Concurrent Dual-Band Low Noise Amplifier for 802.11a/g WLAN applications", IEEE International Conference on Electronics, Circuits and Systems (ICECS), Vol. 1, pp. 66-69, 2006

[20] V. Vidojkovic; J. van der Tang; E. Hanssen; A. Leeuwenburgh; A. van Roermund, "Fully-integrated DECT/Bluetooth multi-band LNA in 0.18 µm CMOS", International Symposium on Circuits and Systems (ISCAS), Vol. I, pp. I-565-568, 2004

[21] Hyejeong Song; Huijung Kim; Kichon Han; Jinsung Choi; Changjoon Park; Bumman Kim, "A Sub-2 dB NF Dual-Band CMOS LNA for CDMA_WCDMA Applications", IEEE Microwave and Wireless Components Letters, Vol. 18, No. 3, pp. 212-214, 2008

[22] Balemarthy, D.; Paily, R., "Process Variations and Noise Analysis on a Miller Capacitance Tuned 1.8_2.4-GHz Dual-Band Low Noise", IEEE International Conference on Advances in Computing, Control & Telecommunication technology (ACT), pp. 414-418, 2009

[23] Datta, K.; Datta, R.; Dutta, A.; Bhattacharyya, T.K., "PSO optimized concurrent dual-band LNA with RF switch for better inter-band isolation", European Conference on Circuits and Systems for Communications (ECCSC), pp. 59-62, 2010

[24] Anh Tuan Phan; Farrell, R., "Reconfigurable multiband multimode LNA for LTE/GSM, WiMAX, and IEEE 802.11.a/b/g/n", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp. 78-81, 2010

[25] Vu Kien Dao; Byoung Gun Choi; Chul Soon Park, "Dual-band LNA for 2.4/5.2GHz applications", Asia-Pacific Microwave Conference, Vol. I, pp. 413-416, 2006

[26] Dao, Vu Kien; Choi, Byoung Gun; Park, Chul Soon, "A Dual-band CMOS RF Front-end for 2.4/5.2 GHz Applications", IEEE Radio and Wireless Symposium, Vol. I, pp. 145-148, 2007

[27] Hongrui Wang; Dajie Zeng; Dongxu Yang; Li Zhang; Yan Wang; Zhiping Yu, "A switchable dual-band LNA with simultaneous noise and input impedance matching for GSM/TD-SCDMA applications", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 767-769, 2010

[28] Ragheb, T.; Nejati, H.; Nieuwoudt, A.; Massoud, Y., "Parasitic-Aware Analytical Modeling of Fully Integrated Switchable Narrow-Band CMOS Low Noise Amplifiers", IEEE Annual Wireless and Microwave Technology Conference, pp. 1-5, 2006

[29] Lavasani, S.H.M.; Chaudhuri, B.; Kiaei, S., "A pseudo-concurrent 0.18 µm multi-band CMOS LNA", IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 695-698, 2003

[30] Datta, S.; Datta, K.; Dutta, A.; Bhattacharyya, T.K., "Pseudo Concurrent Quad-Band LNA Operating in 900 MHz/1.8 GHz and 900 MHz/2.4 GHz Bands for Multi-standard Wireless Receiver", International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom), pp. 25-29, 2010

[31] Chun-Hung Wu; Jeng-Rern Yang, "A switchable single_double-band low noise amplifier", International Conference on Computer Research and Development (ICCRD), pp. 266-269, 2011

[32] El-Nozahi, M.; Sanchez-Sinencio, E.; Entesari, K., "A CMOS Low-Noise Amplifier With Reconfigurable Input Matching Network", IEEE Transactions on Microwave Theory and Techniques, Vol. 57, No. 5, Part 1, pp. 1054-1062, 2009