DEVELOPMENTS IN CLOCK AND DATA RECOVERY CIRCUITS FOR PASSIVE OPTICAL NETWORKS

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The demand for higher bandwidth capacity in telecommunication networks is growing continuously, but scaling up the frequency directly has a severe impact on the receiver circuit complexity and, hence, power consumption. Furthermore, although passive optical networks (PONs) are considered as a cost effective solution, further increasing the data-rate is limited by optical signal to noise ratio (OSNR) as dispersion reduces the signal quality. Traditional methods such as stacking wavelengths at lower bit-rates, increase the receiver complexity and cost. On the other hand, when tackling the problem at an architectural level, new opportunities arise.

Firstly, traditional PON end user receivers process the complete aggregated line rate before deciding whether the transmitted packet was destined for the user in case. As such, it is clear that while only using a small fraction of the transmitted data, a lot of power is wasted processing the complete data stream. Sleep modes can reduce the power consumption, but more intelligent time-sharing mechanisms, such as bit interleaving could be employed. Bit-interleaving the PON stream (BiPON) allows the end-user to subsample the incoming data and directly extract the user data. This immensely simplifies the subsequent data processing, and hence allows to incorporate more complex error protection mechanisms. Since only user data is sampled and processed, power consumption directly scales with the user data rate and no longer with the aggregated line rate. To maximally exploit the power reduction of subsampling the incoming bitstream, an intelligent CDR closely integrated with the BiPON protocol is required.

Secondly, although the BiPON protocol enables the use of more complex error protection mechanisms, a further increase of the OSNR by using more complex modulation schemes than the traditionally employed non-return-to-zero transmission is proposed. 3-level duobinary modulation reduces the needed bandwidth to half the bit-rate, allowing the use of cheaper photo-diodes as well as increasing the tolerance towards dispersion. This has implications on the CDR operation: Phase detection should be performed on a duobinary modulated bitstream. Combining these two improvements results in a CDR operating on a subsampled duobinary modulated signal. During this talk, our research in the frame of Greentouch and the EU FP7 project DISCUS, will be discussed in detail.

Guy Torfs was born in Antwerp, Belgium, in 1984. He received the Engineering degree in applied electronics and the Ph.D. degree in applied sciences, electronics from Ghent University, Ghent, Belgium in 2007 and 2012 respectively. Since his graduation, he works as a post-doctoral researcher at the department of information technology (INTEC, associated lab of IMEC). His research focuses on high-speed, high-frequency, mixed signal electronic circuits and systems, and their applications on chip and board level, including RF transceivers for wireless systems and instrumentation, frequency synthesis and clock recovery applications for optical access networks and transceivers for high-speed back plane interconnections.