

# Preliminary Measured Results from a $\beta$ -Encoder Integrated Circuit

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**Abstract**—We show preliminary measured results from a prototype integrated circuit that implements a fully-differential A/D converter circuit based on a scale-adjusted  $\beta$ -expansion with a switched-capacitor integrator as a core building block. The measured results include the A/D conversion characteristics with estimation of the value of  $\beta$ , and characteristics of the binary output sequences when the  $\beta$  A/D converter circuit works as a chaos generator with a  $\beta$ -expansion chaotic attractor.

## 1. Introduction

As an expansion method of a real number with a real number base, a  $\beta$ -expansion has been mathematically studied for many years based on the ergodic theory, number theory and nonlinear dynamics theory. As a circuit implementation of the  $\beta$ -expansion, a  $\beta$ -encoder was proposed [1]. Recently, a  $\beta$ -expansion attractor was defined, and the characteristics of  $\beta$ -encoder were discussed in detail through a  $\beta$ -map [2, 3]. In addition, a scale-adjusted  $\beta$ -map was introduced for a practiced circuit implementation. A scale-adjusted negative  $\beta$ -map was also defined, and an algorithm for the negative  $\beta$ -encoder was proposed [2, 3]. A 2-state Markov chain approximation was used to show that the binary output sequences of the scale-adjusted ordinary and negative  $\beta$ -encoders have a variety of auto-correlation characteristics including a negative one depending on the values of  $\beta$  and threshold.

A series of researches on the practical IC implementation of the  $\beta$ -encoder with 90 nm CMOS technology has demonstrated through experiments its robustness against changes in the value of  $\beta$ , value of threshold voltage, and temperature [5–7]. In addition, a practiced method to estimate the value of  $\beta$  from the observed bit sequences was proposed for IC implementation [4]. On the other hand, theoretical analyses of the  $\beta$ -encoder circuit established a useful design guideline for the  $\beta$ -encoder circuit [8]. Based on these results, a pipelined  $\beta$ -encoder architecture was proposed [9].

As yet another circuit implementation method, especially for laboratory experiments, a switched-capacitor (SC) circuit technique was employed [10, 11]. Through the circuit experiments with discrete components, the ordinary and negative  $\beta$ -expansion attractors were shown. In addition, the characteristics of the binary sequences obtained from these attractors were also investigated. The same SC

circuit techniques were applied to an integrated circuit that can realize both the ordinary and negative  $\beta$ -encoders [12]. A prototype chip for this circuit was implemented with the TSMC 90 nm CMOS process technology [12].

In this paper, we preliminarily evaluate experimentally the characteristics of the prototype IC chip when the circuit operates as the scale-adjusted ordinary  $\beta$ -encoder. In experiments, we evaluate 1) A/D conversion characteristics, and 2) characteristics as a chaotic circuit with the  $\beta$ -expansion attractor.

In section 2, we shortly review the  $\beta$ -encoder [1–3]. In section 3, we explain the fully-differential  $\beta$ -encoder integrated circuit based on the SC integrator, of which we measure characteristics [12]. In section 4, we show the preliminary measured A/D conversion characteristics with different values of  $\beta$ . Finally, in section 5, we demonstrate the auto-correlation characteristics of the binary output sequences obtained from the  $\beta$ -expansion attractor according to the value of  $\beta$ .

## 2. A/D Converter Based on the Scale-Adjusted $\beta$ -Map

The A/D converter based on the scale-adjusted  $\beta$ -map with a conversion radix of  $\beta$  ( $1 < \beta < 2$ ) is defined as [1–3]

$$x_{(t_{n+1})} = \begin{cases} \beta x_{(t_n)}, & x_{(t_n)} \in [0, \gamma\nu), \\ \beta x_{(t_n)} - s(\beta - 1), & x_{(t_n)} \in [\gamma\nu, s), \end{cases} \quad (1)$$

where  $t_n$  is a discrete time ( $n = 1, 2, \dots$ ),  $\nu \in [s(\beta - 1), s]$  is a threshold parameter,  $s > 0$  is a scaling parameter, and  $\gamma = 1/\beta$ . Moreover, a quantization function  $Q_\theta(x_{(t_n)})$  is given as

$$Q_\theta(x_{(t_n)}) = \begin{cases} 0, & x_{(t_n)} \in [0, \theta), \\ 1, & x_{(t_n)} \in [\theta, s), \end{cases} \quad (2)$$

where  $\theta = \gamma\nu$  is a threshold of the quantization. As a result, a binary sequence  $b_{(t_n)}$  can be defined as

$$b_{(t_n)} = Q_\theta(x_{(t_n)}). \quad (3)$$

By using Eqs. (2) and (3), we can rewrite Eq. (1) as

$$x_{(t_{n+1})} = \beta x_{(t_n)} - b_{(t_n)}s(\beta - 1). \quad (4)$$

The tolerable range of the value of threshold is given as [2, 3]

$$\theta \in [s(1 - \gamma), s\gamma]. \quad (5)$$

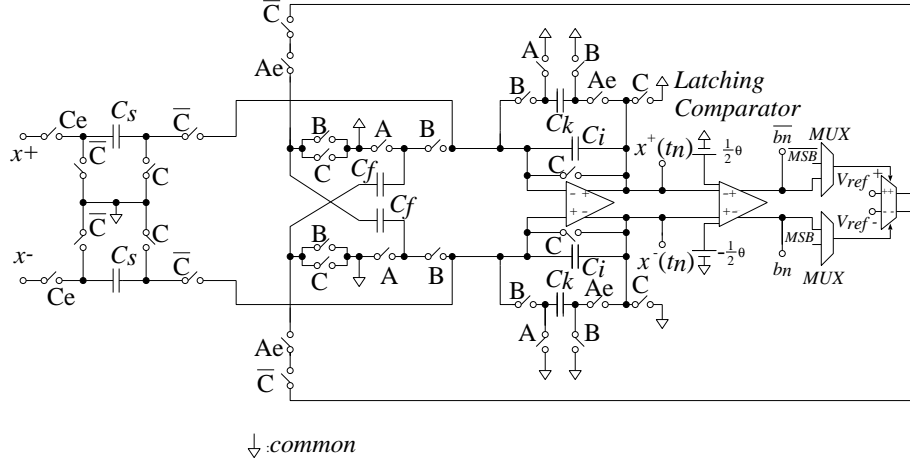


Figure 1: The fully-differential A/D converter circuit based on the scale-adjusted  $\beta$ -map with a SC integrator implemented in the prototype chip.

### 3. The A/D Converter Integrated Circuit Based on the Scale-Adjusted $\beta$ -Map with a SC Integrator.

The A/D converter circuit based on the scale-adjusted  $\beta$ -map with a SC integrator implemented in the prototype chip is shown in Fig. 1 [12].

The circuit operates with non-overlapping clocks A and B, and a reset clock C. In addition to these main clocks, auxiliary clocks Ae and Ce are used, which go high a little earlier than A and C, respectively, to prevent the outflow of charges.

All the capacitors in the circuit are realized as programmable capacitive arrays (PCAs), so that we can change the value of  $\beta$  by properly setting the values of PCAs according to Eq. (6).

$$\begin{aligned} \frac{C_s}{C_i} &= 1, \\ \frac{C_f}{C_i} + 1 &= \beta, \\ \frac{C_k}{C_i} + 1 &= \beta. \end{aligned} \quad (6)$$

The  $\beta$ -map for  $x(t_n) = x^+(t_n) - x^-(t_n)$  realized with the fully-differential circuit in Fig. 1 is shown in Fig. 2, when  $V_{ref} = V_{ref}^+ - V_{ref}^- = 1$ , and  $\theta = 0$ . As shown in the figure, Eq. (1) can be rewritten as

$$\begin{aligned} x(t_{n+1}) &= x^+(t_{n+1}) - x^-(t_{n+1}), \\ &= \begin{cases} \beta x(t_n) + V_{ref}(\beta + 1), & x(t_n) \in [0, \theta), \\ \beta x(t_n) - V_{ref}(\beta - 1), & x(t_n) \in [\theta, s). \end{cases} \end{aligned} \quad (7)$$

In this case, the tolerable range of the threshold is given as

$$\theta \in [V_{ref}(-2\gamma + 1), V_{ref}(2\gamma - 1)]. \quad (8)$$

### 4. A/D Conversion Characteristics

In this section, we evaluate the A/D conversion characteristics of the circuit in Fig. 1. We first estimate an effective

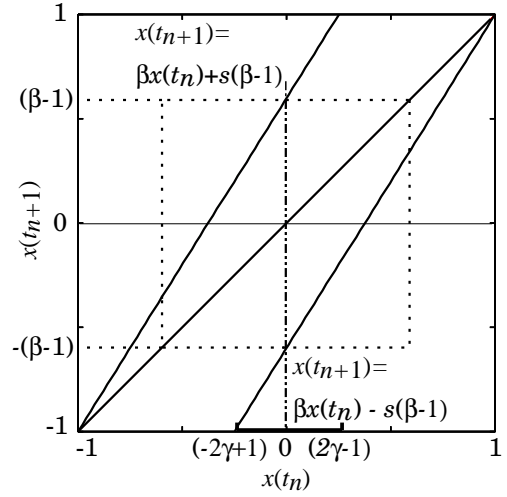


Figure 2: An example of the  $\beta$ -map for  $x(t_n) = x^+(t_n) - x^-(t_n)$  realized by the fully-differential circuit in Fig. 1, when  $V_{ref} = V_{ref}^+ - V_{ref}^- = 1$ , and  $\theta = 0$ .

value of  $\beta$  realized by the circuit using the estimation method suitable for circuit implementation proposed in [4]. The estimation algorithm is based on the fact that the value of  $e(\beta)$  given below should be 0 when the estimated value of  $\beta$  is equal to the real value.

$$e(\beta) = \sum_{i=1}^{\infty} (b_0(t_i) - b_1(t_i)) \cdot \beta^{-i} \quad (9)$$

where  $b_0(t_i)$  and  $b_1(t_i)$  are bit sequences when the MSBs of each bit sequences are 0 and 1, respectively, when we set  $x^+(t_0) = x^-(t_0)$  (the inputs are shorted), and  $\theta = 0$  V.

We estimated the values of  $\beta$  when we set the PCA to obtain the values of  $\beta$  from 1.1 to 1.9841 (designed values). The bit length used for the estimation was 20 when the designed values of  $\beta$  are more than 1.4, while it was 40

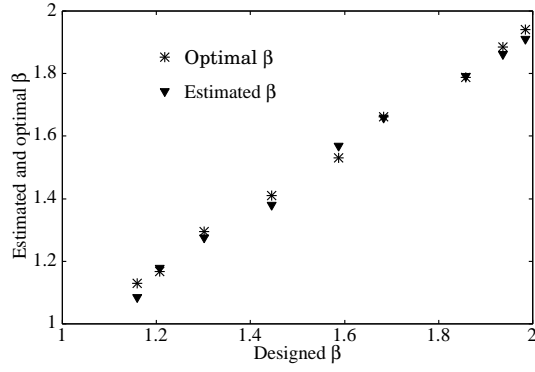


Figure 3: The estimated and optimal values of  $\beta$  vs. the designed values of  $\beta$  (preliminary).

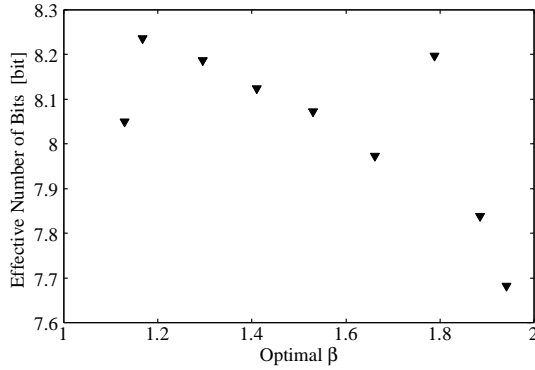


Figure 4: ENOB vs. the optimal values of  $\beta$  (preliminary).

otherwise.

Next, we measured the effective number of bits (ENOBs) of the circuit shown in Fig. 1 with the designed values of  $\beta$  of 1.1 to 1.9841. We then derived the optimal values of  $\beta$  with which the circuit gives the best ENOBs.

Figure 3 shows the estimated values of  $\beta$  from Eq. (9), and the optimal values of  $\beta$  obtained from the ENOBs for several designed values of  $\beta$ . Figure 4 shows the measured ENOBs for different optimal values of  $\beta$ .

## 5. Characteristics of the Binary Output Sequences

The circuit in Fig. 1 can be used as a chaos generating circuit [12]. In this section, we evaluate characteristics of the binary output sequences experimentally obtained from the circuit in Fig. 1.

Since the circuit in Fig. 1 is a fully-differential circuit with the  $\beta$ -map shown in Fig. 2, the transition probabilities are defined as

$$\begin{aligned} A &= \Pr[b(t_{n+1}) = 1 | b(t_n) = 0] \\ &= \frac{\theta - \{\gamma\theta - \gamma s(\beta - 1)\}}{\theta - \{\nu - s(\beta - 1)\}}, \\ B &= \Pr[b(t_{n+1}) = 0 | b(t_n) = 0] = 1 - A, \\ C &= \Pr[b(t_{n+1}) = 0 | b(t_n) = 1] \end{aligned}$$

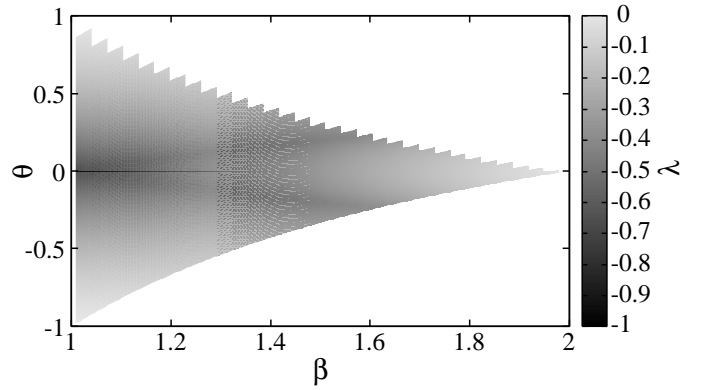


Figure 5: The second eigenvalues  $\lambda$  obtained from the numerical simulation for different values of  $\beta$  and  $\theta$ .

$$\begin{aligned} &= \frac{\gamma\theta + \gamma s(\beta - 1) - \theta}{\nu + s(\beta - 1) - \theta}, \\ D &= \Pr[b(t_{n+1}) = 1 | b(t_n) = 1] = 1 - C. \end{aligned} \quad (10)$$

Given A, B, C, and D above, the transition probability matrix  $P_{\beta,\nu}$  is given by

$$P_{\beta,\nu} = \begin{cases} \begin{pmatrix} B & A \\ 1 & 0 \end{pmatrix} & \text{for } \nu < \nu_a, \\ \begin{pmatrix} B & A \\ C & D \end{pmatrix} & \text{for } \nu_a \leq \nu \leq \nu_b, \\ \begin{pmatrix} 0 & 1 \\ C & D \end{pmatrix} & \text{for } \nu > \nu_b, \end{cases} \quad (11)$$

where

$$\begin{aligned} \nu_a &= \frac{s(\beta - 1) - s\gamma(\beta - 1)}{\gamma^2 - 1}, \\ \nu_b &= \frac{s(\beta - 1) - s\gamma(\beta - 1)}{-\gamma^2 + 1}. \end{aligned} \quad (12)$$

The results of the numerical simulations with Eqs. (10) to (12) are shown in Fig. 5. In the simulations, the value of  $\beta$  was varied from 1.01587 to 1.9841 in steps of  $2^{-5}$ , while  $V_{ref} = 1$  V. In addition, the value of  $\theta$  was changed in steps of 0.01 V.

To estimate the second eigenvalue from the experimentally obtained binary sequence,  $b(t_1), b(t_2), b(t_3), \dots, b(t_L)$ , we approximate the sequence by using the 2-state Markov chain with a transition matrix  $P^{frequency}$  as [2],

$$P^{frequency} = \begin{pmatrix} \frac{n_{00}}{n_{00} + n_{01}} & \frac{n_{01}}{n_{00} + n_{01}} \\ \frac{n_{10}}{n_{10} + n_{11}} & \frac{n_{11}}{n_{10} + n_{11}} \end{pmatrix}, \quad (13)$$

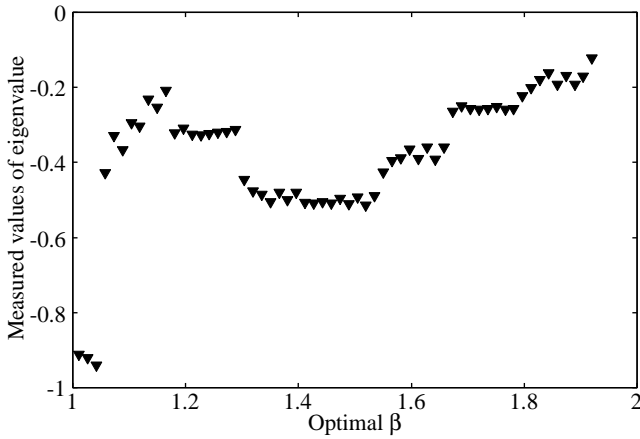


Figure 6: The experimentally obtained second eigenvalues through the 2-state Markov chain approximation (preliminary).

where  $n_{00}$ ,  $n_{01}$ ,  $n_{10}$ , and  $n_{11}$  are frequencies defined as

$$\begin{aligned} n_{00} &= \sum_{i=1}^{L-1} \overline{b(t_i)} \cdot \overline{b(t_{i+1})}, & n_{01} &= \sum_{i=1}^{L-1} \overline{b(t_i)} \cdot b(t_{i+1}), \\ n_{10} &= \sum_{i=1}^{L-1} b(t_i) \cdot \overline{b(t_{i+1})}, & n_{11} &= \sum_{i=1}^{L-1} b(t_i) \cdot b(t_{i+1}), \end{aligned} \quad (14)$$

where  $L$  is the length of the bit sequence.

In the circuit experiments, we use  $L = 100000$ , and  $V_{ref} = 1$  V, while the value of  $\beta$  was varied from 1.095323 to 1.9841 with optimal  $\beta$ . The threshold voltage of the quantizer was 0 V. The result is shown in Fig. 6. From this result, we confirm that we can easily obtain negative eigenvalues, which are useful for some engineering applications.

## 6. Conclusions

In this paper, we measured the prototype A/D converter integrated circuit based on the scale-adjusted  $\beta$ -map with the SC integrator. The preliminary results for the conversion characteristics has been shown. In addition, we evaluated the prototype circuit as the chaotic circuit by using the eigenvalues of the output bit sequences.

Because these results are preliminary, some deviations from the theory were observed. We already found out that the clock waveforms are not good enough for precise measurements. Therefore, we will further improve the measurements to obtain better results. Furthermore, we will confirm the robustness of the  $\beta$ -encoder circuit against circuit parameter values and temperature.

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