# Qualitative Behavior for Simple H-Bridge Inverter

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**Abstract**—In this paper, we investigate the qualitative behavior of the PWM current-controlled H-bridge inverter with the periodic external forces. First, we show the circuit model with the sinusoidal wave and a clock pulse as the periodic external forces and explain its dynamics. Then, we define the discrete map and numerically calculate the bifurcation diagrams in the circuit. Finally, we discuss the qualitative behavior of the PWM current-controlled H-bridge inverter.

## 1. Introduction

The interrupted dynamical system is dependent on the state and periodic interval. The power conversion circuits such as the dc/dc converter and dc/ac inverter are the typical example of the interrupted dynamical system and these are used in the electrical engineering field. Also, the complex switching action causes rich nonlinear phenomena. Many researchers have investigated these phenomena in a long term [1–4].

There is the pulse width modulation (PWM) technique as one of the control methods of the power conversion circuit [5, 6]. Switching of the state is determined by comparing the output signal of the collector and carrier signal. Further, sinusoidal wave and a clock pulse are impressed the control circuit. Accordingly, the circuit with PWM controller shows the various oscillations depending on the carrier signal and sinusoidal wave are applied to the collector. In general, the oscillations, which observe in the short and long-period are called the fast-scale and slow-scale dynamics respectively. In previous works, the relationship between the fast-scale and slow-scale dynamics has not been discussed. So, Ref. [7] reported that fast-scale and slow-scale dynamics interacts under certain conditions. However, Ref. [7] discussed the fast-scale and slow-scale dynamics in current-controlled dc/dc converter. There are few litterateurs discussed the relationship between the fast-scale and slow-scale dynamics of the dc/ac inverter with the PWM controller.

In this paper, we investigate the circuit model, which is improved circuit shown in [8, 9] with the fast-scale and slow-scale dynamics as the first step to study qualitative behavior in the dc/ac inverter. First, we show the circuit model and explain its dynamics. Then, we define the discrete map and numerically calculate the bifurcation diagrams. Finally, we investigate the qualitative behavior of the circuit.

## 2. Simple H-bridge inverter

### 2.1. Circuit dynamics

Figure 1 shows a simple PWM current-controlled H-bridge inverter. We set the circuit parameters as $E = 400$[V], $R = 40[\Omega]$, $L = 20$[mH] [8, 9]. The circuit model has a PWM modulator with a proportional corrector. In the circuit, we applied the inductance current, which is discretized every period of the clock pulse, and reference current to the collector. Then, the reference current $I_r$ is defined as $I_r = i_r + A \sin \omega t$. Also, we define the variable $\omega = 2\pi/(NT_c)$ and fix $N = 50$. In particular, the case of $A = 0.0$ is studied in [8, 9]. In the following analysis, $T_c$ and $T_s = 2\pi/\omega$ are denoted the period of the clock pulse and the sinusoidal wave, respectively. Accordingly, the corrector outputs the control voltage $u_n$ as follows:

$$u_n = k(I_r - i_n), \qquad k > 0, \tag{1}$$

where $k$ denotes the ratio of amplifier. Besides, the circuit consists of four switches, and we denote them as SW1, SW2, SW3 and SW4. Now, the switching state can be divided into two types. The switches SW1 and SW2 are open and SW3 and SW4 are close for system-a. Also, the switches SW1 and SW2 are close and SW3 and SW4 are open for system-b. The circuit equations corresponding to

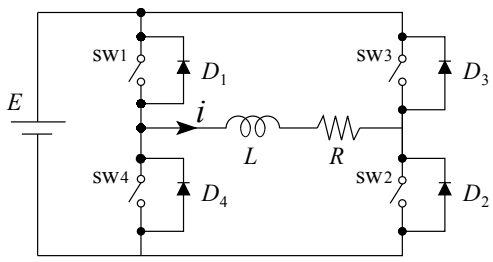



Figure 1: Circuit model.

each state are given by

$$L\frac{di}{dt} = \begin{cases} -Ri - E & : \text{system-a} \\ -Ri + E & : \text{system-b} \end{cases}. \tag{2}$$

We use the dimensionless value $\tau = Rt/(2L)$ in the following analysis. Similarly, the clock pulse and sinusoidal wave interval are $T'_c = RT_c/(2L)$ and $T'_s = RT_s/(2L)$. Then, we rewrite $T'_c$ and $T'_s$ as $T_c$ and $T_s$. Figure 2 shows the proportional corrector and PWM modulator. The output of the PWM modulator $\mathrm{sat}(u_n)$ is defined as follows:

$$\mathrm{sat}(u_n) = \begin{cases} -1, & u_n \le -1 \\ u_n, & -1 < u_n < 1 \\ 1, & u_n \ge 1 \end{cases}. \tag{3}$$

Moreover, we define the duty ratio $D_n$, which depend on the output of PWM controller as follows:

$$D_n = \frac{1}{2} + \frac{\mathrm{sat}(u_n)}{2}. \tag{4}$$

We show an example of the waveform in Fig. 3. Behavior of the waveform during the clock interval is divided into three types depends on $u_n$. If the value of $u_n$ satisfies $u_n \le -1$ (or $1 \le u_n$) the state of the switches during a clock interval keeps system-a (or b). On the other hand, if the value of $u_n$ satisfies $-1 < u_n < 1$, the state of the switches during a clock interval is shifts from system-a to b, and then it returns to system-a. Now, during a time $\tau_a$ and $\tau_b$, state keeps system-a and system-b are defined as follows:

$$\tau_a = \frac{(1 - D_n)}{2}T_c, \qquad \tau_b = D_n T_c. \tag{5}$$

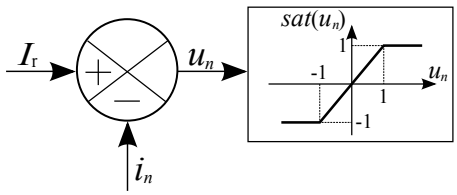



Figure 2: Proportional corrector and PWM modulator.

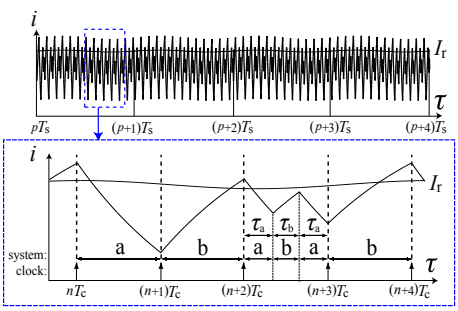



Figure 3: Example of the waveform.

### 2.2. Discrete map

We sampled the waveform at every period of $T_c$ and $T_s$ in order to define the discrete map of the circuit. Here, the reference current is defined as $I_r = i_r + A\sin n\omega t$. Also, the variable $n$ is $n = 0, 1, 2, ..., N-1$ and we let $i_n$ be a solution at the time $\tau = nT_c$. In particular, we define the solution at the time $\tau = 0$ and $\tau = NT_c$ are $i_p$ and $i_{p+1}$ respectively. Then, the discrete map of slow-scale dynamics is defined as follows:

$$\begin{aligned} i_{p+1} &= F(i_p) \\ &= F_{N-1} \circ \ldots \circ F_n \circ \ldots \circ F_1 \circ F_0(i_p). \end{aligned} \tag{6}$$

In Eq. (6), $F_n$ means the discrete map of fast-scale dynamics. Figure 4 shows the conceptual diagram of the discrete map in fast-scale dynamics. Based on the solutions of Eqs. (2) and (5), the discrete map of fast-scale dynamics is defined as follows:

$$F_n(i_n) = i_{n+1} = \begin{cases} i_n e^{-2T_c} + 2\dfrac{E}{R}T_c e^{-T_c}, & i_n \le C_1(n) \\ \left(e^{-2T_c} - 2k\dfrac{E}{R}T_c e^{-T_c}\right)i_n \\ \qquad +2k\dfrac{E}{R}T_c e^{-T_c}\left(i_r + A\sin n\omega T_c\right), \\ \qquad C_2(n) < i_n < C_1(n) \\ i_n e^{-2T_c} - 2\dfrac{E}{R}T_c e^{-T_c}, & i_n \ge C_2(n) \end{cases}. \tag{7}$$

In Eq. (7), $C_1(n)$ and $C_2(n)$ are borders for classifying three types of the waveform in Fig. 4, which are expressed in the following equation.

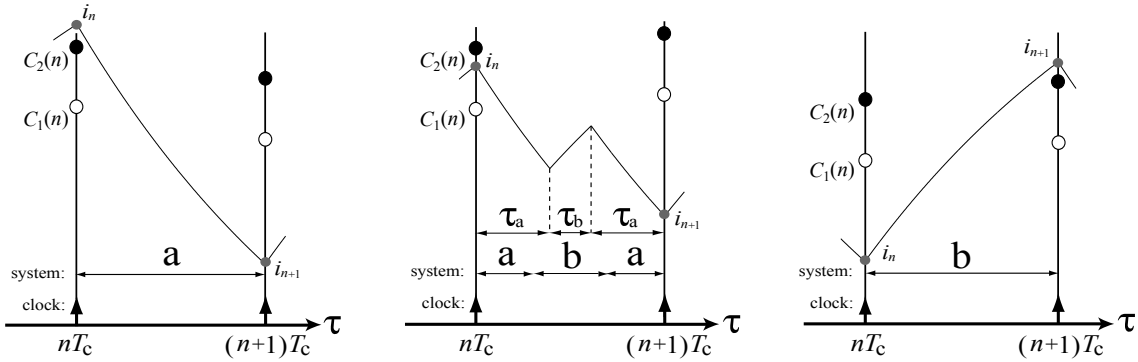
$$\begin{aligned} C_1(n) &= i_r + A\sin n\omega T_c - \frac{1}{k}, \\ C_2(n) &= i_r + A\sin n\omega T_c + \frac{1}{k}. \end{aligned} \tag{8}$$

## 3. Analytical results

In the following analysis, the circuit parameters are fixed as:

$$k = 1.2,\ T_s = 15,\ T_c = 0.3. \tag{9}$$

Figure 5 shows the one-parameter bifurcation diagram and the corresponding Lyapunov exponent. It can be seen from Fig. 5 that bifurcation phenomena occurs with changing the parameter $i_r$. For example, the period-1 solution bifurcates to the period-2 solution around $i_r = 2.0$. Then, the period-2 solution bifurcates to the chaotic attractor around $i_r = 4.0$. After that, chaotic attractor is obtained again through the period-3 solution. In Fig. 6, we show the waveform and discrete map of the slow-scale dynamics as $i_r = 6.4$ and $i_r = 6.6$. From these figures, we can see the state of fast-scale and slow-scale dynamics is stable at

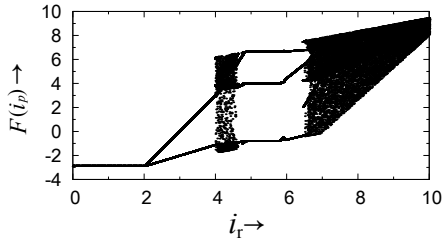



(a) $u_n \leq -1$ (b) $-1 < u_n < 1$ (c) $u_n \geq 1$

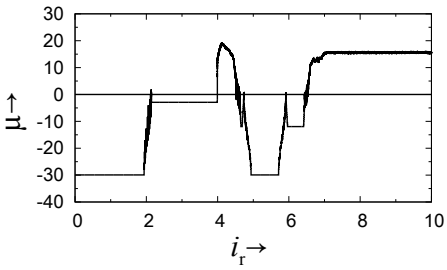
Figure 4: Classified waveform during the clock interval $T_c$.

$i_r = 6.4$. However, we consider that bifurcation phenomena occurred in fast-scale dynamics makes behavior of the slow-scale dynamics unstable. In our previous works, we analyzed the border-collision bifurcation in interrupted circuit with fast-scale and slow-scale dynamics. In Ref. [4], we showed that border-collision bifurcation causes fast-scale and slow-scale dynamics to destabilized at the same time. Therefore, we consider the same phenomenon has occurred through the border-collision bifurcation around the $i_r = 6.5$ from Fig. 6.

If we set the parameter of amplitude $A = 0.0$, we can obtain the equivalent circuit model in [8, 9]. In the following analysis, we compare the case of amplitude $A = 0.0$ with $A = 0.1$ to discuss the qualitative behavior of the circuit. Figure 7 shows the one-parameter bifurcation diagram of the circuit and the corresponding Lyapunov exponent

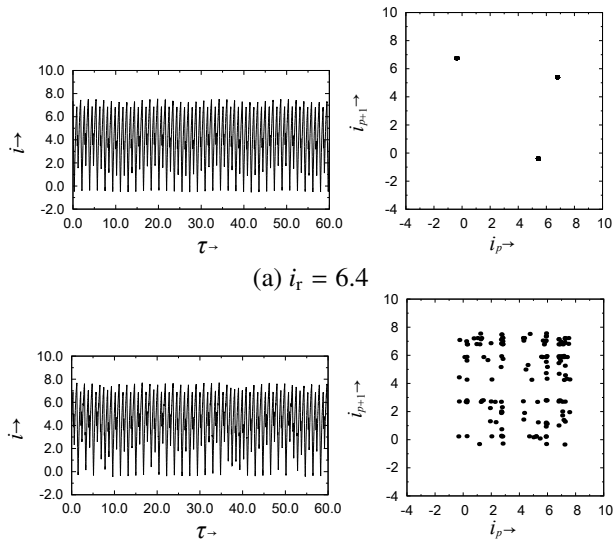



(a) One-parameter bifurcation diagram




(b) Lyapunov exponent

Figure 5: One-parameter bifurcation diagram and Lyapunov exponent. ($A = 0.1, T_c = 0.3$)

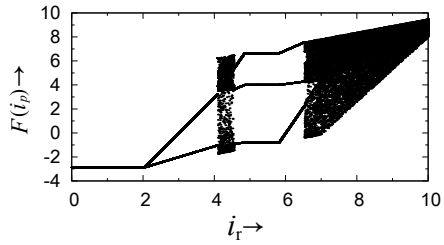



(a) $i_r = 6.4$

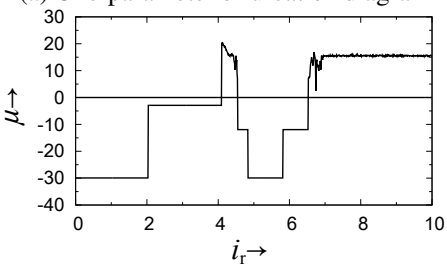
(b) $i_r = 6.6$

Figure 6: Border-collision bifurcation. ($A = 0.1, T_c = 0.3$)

at $T_c = 0.3$ and $A = 0.0$. Moreover, we show the two-parameter bifurcation diagrams in Fig. 8. The bifurcation parameters are the reference value $i_r$ for the $x$-axis and the period of the clock pulse $T_c$ for the $y$-axis, respectively. In Fig. 8, the area of yellow, blue and green correspond to the existence region of the solution and the red area means the over period-4 solution. From these figures, bifurcation structure of the circuit is similar to the case of $A = 0.0$. Here, the amplitude of reference current affects the behavior of the circuit if the control voltage satisfies $-1 < u_n < 1$ (see Eq. (3)). Therefore, we conclude that if the control voltage satisfies $-1 \geq u_n$ or $1 \leq u_n$, the same bifurcation phenomena in [8, 9] occurs. On the other hand, period-3 solution bifurcates to a different period-3 solution around $i_r = 6.0$ in Figs. 5 and 7. Specifically in Fig. 5, the control voltage satisfies $-1 < u_n < 1$ at the period-3 solution of the fast-scale dynamics. Thus, the sinusoidal wave, which is applied to the reference current affecting the behavior of the circuit.




(a) One-parameter bifurcation diagram

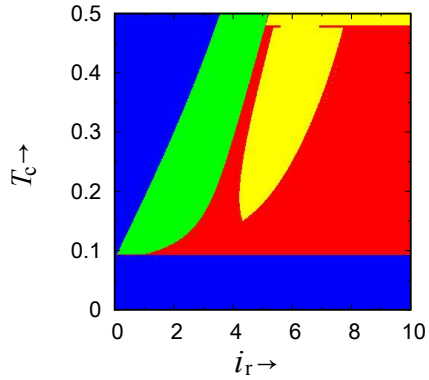



(b) Lyapunov exponent

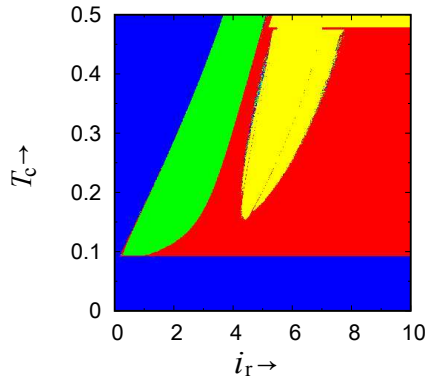
Figure 7: One-parameter bifurcation diagram and Lyapunov exponent. ($A = 0.1, T_c = 0.3$)

## 4. Conclusion

In this paper, we reported nonlinear phenomena in the PWM current-controlled H-bridge inverter. First, the circuit model including sinusoidal wave of the corrector, which produces the PWM signal was shown. Then, we calculated the bifurcation diagrams from the discrete map. Finally, we discussed the qualitative behavior of the circuit. In the circuit, there are fast-scale and slow-scale dynamics depending on the clock pulse and sinusoidal wave, which is applied to the collector. This paper revealed the possibility that slow-scale dynamics becomes unstable with the border-collision bifurcation of the fast-scale dynamics. Implementation of the circuit is the future work.




(a) $A = 0.0$




(b) $A = 0.1$

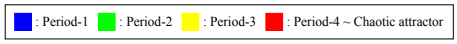



Figure 8: Two-parameter bifurcation diagrams.

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