Multi-phase Synchronization in Interconnected System of Buck Converters

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Abstract— This paper studies multi-phase synchronization in an interconnected system of buck converters with two kinds of switching rules: the clock-based and the winner-take-all-based switching rules. Simplifying the system into a piecewise linear model and applying the mapping procedure, stability and ripple characteristics of the synchronization phenomena are analyzed precisely. Presenting a simple test circuit, typical phenomena are confirmed experimentally.

1. Introduction

The interconnected system of power converters (IPC) have been studied extensively [1]-[4]. The IPC consists of N pieces of single power converters connected by a switching rule. In the IPC, N-phase synchronization (N-SYN) is a key phenomenon. The N-SYN is effective for ripple reduction, fault tolerance and current sharing for low voltage and high current capabilities. The ripple reduction can contribute to reduce size and losses of the filtering stages and to decrease electromagnetic interference levels. The robustness of the parallel operation is effective for high-power operation such as electric vehicles.

This paper studies the N-SYN in an interconnected system of buck converters (IBC). The system is constructed by connecting N buck converters in parallel. The study of the IBC is important not only for practical applications but also as basic nonlinear problems [5]-[9]. In order to realize the parallel connection, we consider two kinds of switching rules: a clock-based switching (SW-CLK) and a winner-take-all (WTA)-based switching (SW-WTA) [10]-[13]. In the SW-CLK, each buck converter (sub-system) is controlled by a common periodic clock and the N-SYN can be realized. The SW-WTA uses periodic current selection based on the WTA principle and can realize the N-SYN automatically. Simplifying the IBC into a piecewise linear model and applying the mapping procedure, stability and ripple characteristics of the N-SYN can be analyzed precisely. It is basic to analysis of the bifurcation phenomena. Presenting a simple test circuit, typical phenomena are confirmed experimentally. It should be noted that our previous publications [10]-[13] do not consider the clock-based switching.

2. Interconnected System of Buck Converters

Figure 1 shows the IBC whose sub-systems share the output current: $i_o \equiv i_1 + \cdots + i_N$. The j-th sub-system can be either of the following two state:

State 1: S_j is conducting and D_j is blocking
State 2: S_j is blocking and D_j is conducting.

where $j = 1 \sim N$. The state transition is defined by either of the following two switching rules.

SW-CLK (Fig. 2 (a)): Let the j-th sub-system be State 2 where the j-th dimensionless current x_j decays. If the x_j reaches the lower threshold X_T then the State 2 is changed

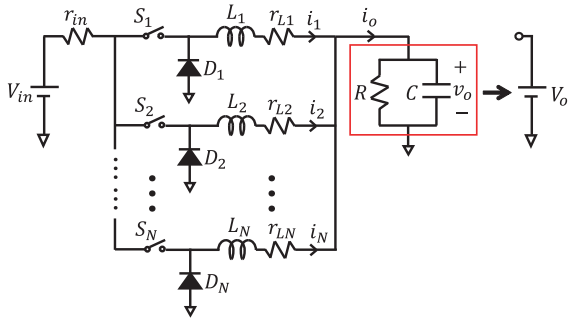

Figure 1: Interconnected system of buck converters.

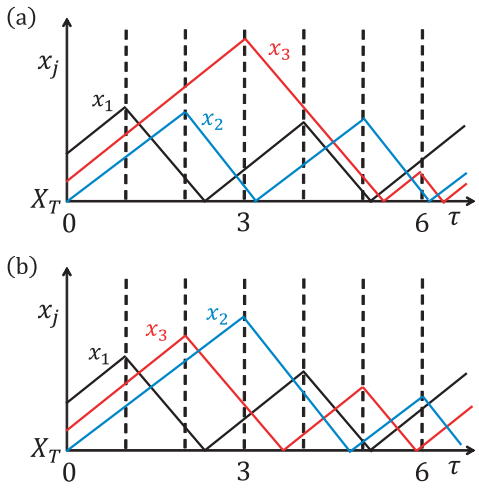

Figure 2: Switching rules: (a) SW-CLK, (b) SW-WTA. τ, x_j, and X_T are proportional to t, i_j and J_T, respectively.

into State 1. The State 1 is changed into State 2 at some clock arriving time $\tau = j + nN$ ($t = jT + nNT$) where T is the basic clock period, $j = 1 \sim N$ and n denotes positive integers. The switching is controlled by the common clock signal with period N and the N-SYN can be realized as discussed afterward.

SW-WTA (Fig. 2 (b)): Switching from State 2 to State 1 is the same as that of the SW-CLK. Let the j-th sub-system be State 1. If the x_j is the maximum among x_1 to x_N at some clock arriving time $\tau = n$ ($t = nT$) then State 1 is changed into State 2. If the j-th sub-system has the maximum current at $\tau = n$ then it is referred to as the winner at $\tau = n$. In this rule, the switching order from State 1 to State 2 (the order of the winner) depends on the initial state and the N-SYN can be realized as discussed afterward.

In order to simplify the analysis, $r_{in} \to 0$ and $RC \to V_o$ where $RC \gg T$ is assumed [10]. The circuit dynamics is described by

$$\frac{dx_j}{d\tau} = \begin{cases} -\alpha_j x_j + a_j & \text{for State 1} \\ -\alpha_j x_j - b_j & \text{for State 2} \end{cases} \tag{1}$$

SW-CLK
State 1 $\to$ State 2 at $\tau = j + nN$
State 2 $\to$ State 1 if $x_j = X_T$

SW-WTA
State 1 $\to$ State 2 if x_j is the maximum at $\tau = n$
State 2 $\to$ State 1 if $x_j = X_T$.

where n denotes positive integers and the following dimensionless variables/parameters are used:

$$\tau = \frac{t}{T},\ x_j = \frac{i_j}{J},\ X_T = \frac{J_T}{J},$$
$$\alpha_j = \frac{Tr_{Lj}}{L_j},\ a_j = \frac{T(V_{in} - V_o)}{L_j J},\ b_j = \frac{TV_o}{L_j J}, \tag{2}$$

where $J_T > 0$ is the lower current threshold, $J > 0$ is a current criterion for a desired operation. Let $x_o = x_1 + \cdots + x_N$ be a dimensionless output current.

For simplicity, we assume that $\alpha_j = \alpha$, $a_j = a$, and $b_j = b$ for $j = 1 \sim N$. Figure 3 shows typical waveforms of the N-SYN. In the SW-CLK, the switching order is controlled by a common clock signal and is fixed. In the SW-WTA, all the combination of the switching order can be realized depending on the initial state.

3. Multi-phase synchronization

First we define the N-SYN.

Definition 1: Let $\boldsymbol{x} = (x_1, \cdots, x_N)$. Let $\{\rho(1), \cdots, \rho(N)\}$ be a permutation of $\{1, \cdots, N\}$. A solution $\boldsymbol{x}(\tau)$ is said to be N-SYN if it is period N and variables x_j share the switching from/to State 1 to/from State 2 during one period.

$$\boldsymbol{x}(\tau + N) = \boldsymbol{x}(\tau),\ x_{\rho(j)+1}(\tau) = x_{\rho(j)}(\tau + 1)$$
$$x_{\rho(j)} \text{ switches from State 1 to State 2 at } \tau = \rho(j) + nN \tag{3}$$

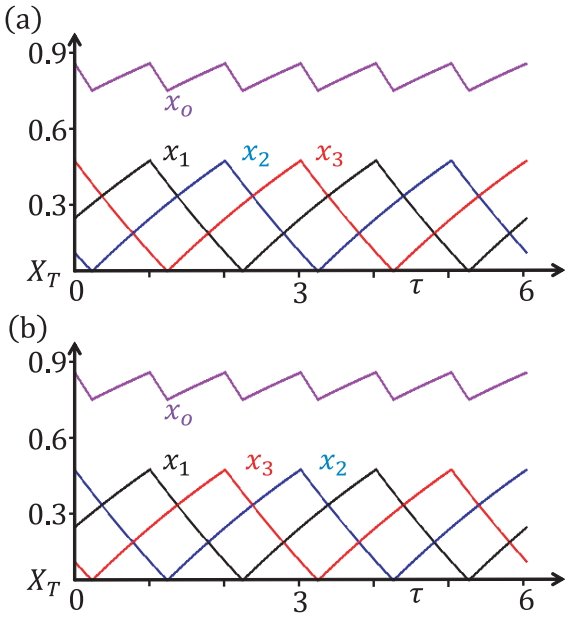

Figure 3: Typical waveforms of the N-SYN for $N = 3$, $\alpha = 0.2$, $a = 0.3$, $b = 0.3$ and $X_T = 0.05$ ($\gamma_R \approx 0.1$). The SW-CLK can realize (a) only because the order of switching is fixed. The SW-WTA can realize both (a) and (b).

Since $\alpha_j = \alpha$, $a_j = a$, $b_j = b$ then the dimensionless output current for the N-SYN satisfies

$$x_o(\tau + 1) = x_o(\tau),\ x_{omin} \equiv x_o(\tau_s) \le x_o(\tau) \le x_o(0) \equiv x_{omax} \tag{4}$$

where τ_s is a phase at which x_j hits the lower thresholds X_T and is switched from State 2 to State 1. Next, we define stability of the N-SYN and ripple factor.

Definition 2: Let $\boldsymbol{x_p} = (x_{1p}, \cdots, x_{Np})$ be a steady state solution of N-SYN. The N-SYN is said to be stable if $\boldsymbol{x}(\tau)$ approaches $\boldsymbol{x}_p(\tau)$ for a small initial perturbation:

$$\boldsymbol{x}(\tau) \to \boldsymbol{x}_p(0) \text{ for } \boldsymbol{x}(0) = \boldsymbol{x}_p(0) + \boldsymbol{\epsilon}(0)$$

Definition 3: In the N-SYN, the ripple of the output current is characterized by the ripple factor

$$\gamma_R = \max_{\tau}(x_o(\tau)) - \min_{\tau}(x_o(\tau)) \quad \text{for } 0 \le \tau < 1. \tag{5}$$

Figure 4 shows ripple factor γ_R of stable N-SYN. $\gamma_R = 0$ (minimum) at $b \approx 0.42$ means that the system exhibits the minimum ripple. As b increases, γ_R of stable N-SYN tends to increases.

Here we consider stability of the N-SYN in the SW-CLK. The N sub-systems are interconnected by the common clock signal and the switching order is fixed. In order to analyze the stability, we employ the mapping procedure. As shown in Fig. 5(a), let $x_n \in L_D$, let $L_D \equiv \{(x_j, \tau) | \text{State 2},\ X_T \le x_j,\ \tau = nN\}$ and let $x_{n+N} \equiv x(n + N)$. Since x_{n+N} is determined by x_n, we can define the return map: $x_{n+N} = f(x_n)$. Using the exact piecewise solution of

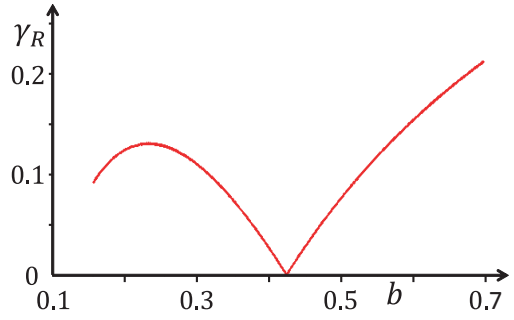

Figure 4: Ripple characteristics for stable N-SYN ($N = 3$, $\alpha = 0.2$, $a = 0.3$ and $X_T = 0.05$).

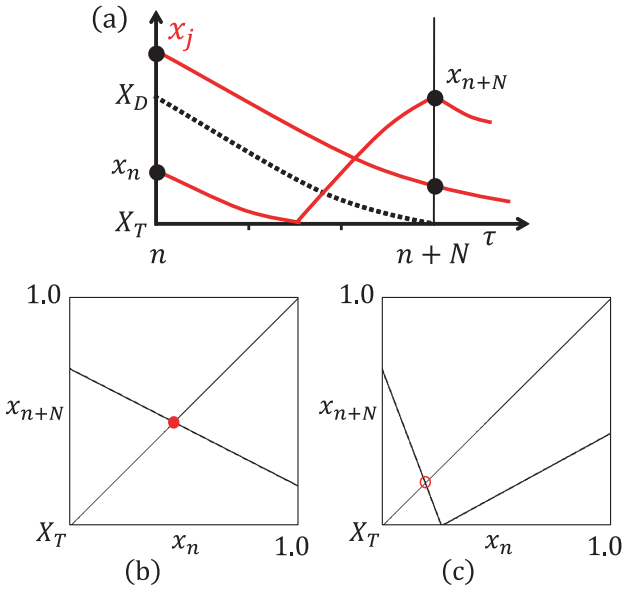

Figure 5: Return map in the SW-CLK. (a) Definition of return map. (b) Stable fixed point for $N = 3$, $\alpha = 0.2$, $a = 0.3$, $b = 0.3$ and $X_T = 0.05$. (c) Unstable fixed point for $N = 3$, $\alpha = 0.2$, $a = 0.3$, $b = 0.05$ and $X_T = 0.05$.

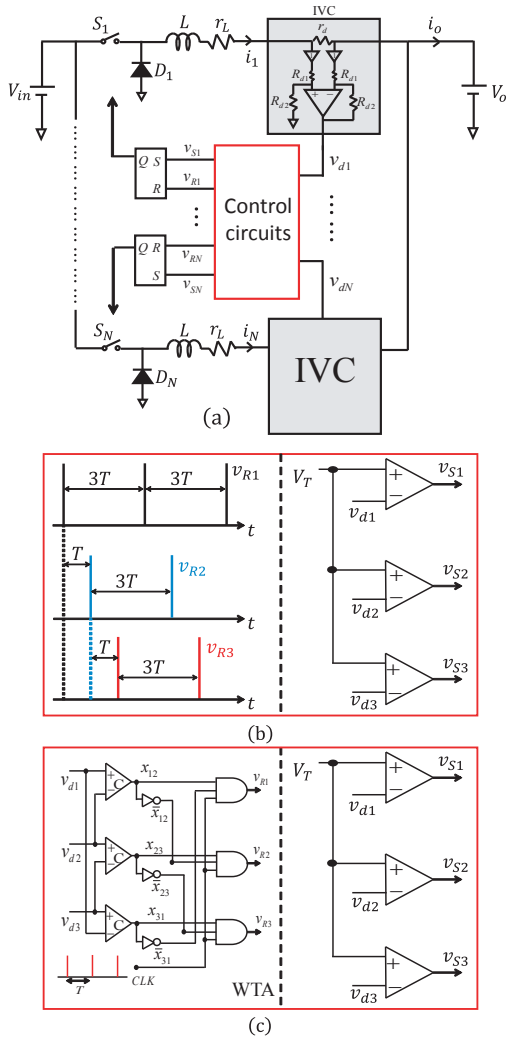

Figure 6: Test circuits for $N = 3$. (a) Equivalent circuits of interconnected system of buck converters. (b) Control circuits for the SW-CLK. (c) Control circuits for the SW-WTA.

Eq. (1), the map can be described exactly:

$$f(x_n) = \begin{cases} e^{-\alpha N}(x_n + p_2) - p_2 & \text{for } X_D < x_n \\ \dfrac{X_T - p_1}{X_T + p_2} e^{-\alpha N}(x_n + p_2) + p_1 & \text{for } x_n \le X_D \end{cases} \tag{6}$$

where $p_1 \equiv a/\alpha > 0$, $p_2 \equiv b/\alpha > 0$, $0 < X_T < p_1$. If the map has a fixed point q as shown in Fig. 5 then the fixed point corresponds to the N-SYN as shown in Fig. 3. If the fixed point is stable then the N-SYN is stable. After simple calculation, we can say that the map has a stable fixed point if

$$\left| \frac{X_T - p_1}{X_T + p_2} e^{-\alpha N} \right| < 1 \tag{7}$$

As the parameter varies, this fixed point becomes unstable and the N-SYN becomes unstable as shown in Fig. 5(c).

In the SW-WTA, N sub-systems are interconnected by the WTA rule and the order of the winner can change. The SW-WTA can realize N-SYN of various order of the switching. The Condition (7) guarantees local stability of the N-SYN in the case where the order of switching is determined. In order to clarify the global stability, more detailed analysis of the domain of attraction is necessary.

4. Laboratory experiments

Figure 6(a) shows test circuits of the IBC. The inductor current is transformed into a voltage via a current-voltage converter (IVC). Output of IVC (v_{dj}) is applied to control circuits. The outputs of the flip-flops control switch S_1 to S_N. Figure 6(b) shows control circuits for the SW-CLK. Switching from State 2 to State 1 is realized by comparing V_T and v_{dj}. The outputs of comparator are applied to set terminal of each flip-flops. Switching from State 1 to State 2 is realized by each clock signal whose period is $3T$ and

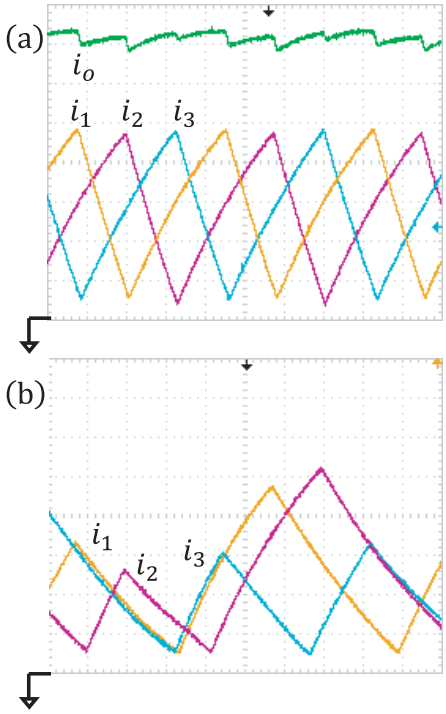

Figure 7: Observed waveforms for $L \approx 100$[mH], $r_L \approx 110[\Omega]$, $r_d \approx 51[\Omega]$, $R_{d1} \approx 1$[kΩ], $R_{d2} \approx 20$[kΩ], $J_T \approx 0.5$[mA] and $T \approx 125[\mu s]$ (Horizontal: 100[μs/div], Vertical: 1[mA/div]). (a) N-SYN in the SW-CLK ($V_{in} \approx 4.8$[V] and $V_o \approx 2.0$[V]). (b) Hyperchaos in the SW-WTA ($V_{in} \approx 2.9$[V] and $V_o \approx 0.4$[V]).

phase shift T. Each clock signal connected to reset terminal of each flip-flops. Figure 6(c) shows control circuits for the SW-WTA. Switching from State 2 to State 1 is realized by the same circuits as the SW-CLK. The WTA function is realized through comparators and logical gates. The outputs of the WTA and comparators are applied to set and reset terminals of each flip-flops, respectively.

Figure 7(a) shows example of the N-SYN in the SW-CLK. As the parameter varies, the N-SYN becomes unstable and chaotic orbit appears. Figure 7(b) shows hyperchaotic phenomenon in the SW-WTA.

5. Conclusions

The N-SYN in a simplified model of the IBC is studied in this paper. Applying the mapping procedure in the case of the SW-CLK, a sufficient condition of parameters for stable N-SYN is given. This condition can guarantee local stability of the N-SYN in the SW-WTA. Typical ripple characteristics of the N-SYN are also demonstrated. Presenting a simple test circuit, typical phenomena are confirmed experimentally. Future problems include stability analysis of the N-SYN in wider parameter range, analysis of bifurcation phenomena and application to a wider class of interconnected switching power converters.

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