Balanced Sub-1-V MOSFET Colpitts-VCO with Varactor-Integrated Feedback Capacitors

#Man-Young Jeon [1], Woon-Suek Baek [2], Ha-Woon Lee [3], Young-Ki Cho [4]
[1] School of Information and Communications, Dongyang Universiy
Yeongju, Kyungpook 750-711, South Korea, myjeon@dyu.ac.kr
[2] School of Information and Communications, Dongyang Universiy
Yeongju, Kyungpook 750-711, South Korea, wsbaek@dyu.ac.kr
[3] School of Information and Communications, Dongyang Universiy
Yeongju, Kyungpook 750-711, South Korea, hwlee@dyu.ac.kr
[4] School of Electronics Engineering, Kyungpook National University
Daegu 702-701, South Korea, ykcho@ee.knu.ac.kr

Abstract

This study integrates a MOS varactor into one of feedback capacitors in the half circuit of a balanced Colpitts VCO. This leads to significant increase of the negative resistance of the balanced Colpitts VCO, thereby ensuring stable start-up of oscillation even at the sub-1-V supply voltage and causing further signal swing in the tank.

Keywords : VCO Balanced VCO MOSFET VCO

1. Introduction

Maintaining or improving voltage controlled oscillator (VCO) performance with shrinking supply voltages dictated by technology scaling imposes a significant design challenge due to signal swing limitations [1]-[2]. The reduced signal swing in turn deteriorates the phase noise since the phase noise is inversely proportional to signal amplitude, which is bound to the supply voltage [3].

Recently, balanced Colpitts-VCOs which can overcome the signal swing limitations were proposed [1], [4]. Those VCOs employ inductors as current sources to resolve the signal swing limitations forced by the sub-1-V supply voltages. At the sub-1-V supply voltage, however, they may suffer from the poor start-up of oscillation which is one of the well known shortcomings of the Colpitts-VCO and its variants [5]. In order to overcome the problem, in addition to using inductor current sources, the balanced Colpitts-VCO proposed by this work employs varactor-integrated feedback capacitor, which integrates the MOS varactor in the individual half circuit of the conventional balanced Colpitts-VCO into one of two feedback capacitors in the half circuit. According to simulations using a 0.18 μm RF CMOS technology, employing the varactor-integrated feedback capacitor significantly increases the negative resistance seen by the equivalent tank inductor, which in turn ensures stable start-up of oscillation and causes further signal swing in tank. In the next Section, negative resistances exhibited by the proposed and conventional VCO will be compared by simulations.

2. Proposed VCO Circuits and Its Negative Resistance

A conventional balanced Colpitts-VCO which employs inductor current sources like [1] but adopts series-tuned tank is shown in Fig. 1(a). We can see the left and right MOS varactors C_{V1} and C_{V2} reside apart from the pairs of feedback capacitors (C_{F1}-C_{F2} and C_{F3}-C_{F4}). The proposed VCO shown in Fig. 1(b) employs inductor current sources like the balanced Colpitts-VCO shown in Fig. 1(a). However, it integrates the MOS varactors C_{V1} and C_{V2} in Fig. 1(a) into their corresponding feedback capacitors C_{F2} and C_{F4}. The circuit with the resultant varactor-integrated feedback capacitors C_{VF2} and C_{VF4} is our proposed balanced Colpitts-VCO shown in Fig. 1(b).

By merging the MOS varactors into feedback capacitors, the proposed VCO further

increases negative resistances seen by tank inductor L_s. Fig. 1(c) shows the half circuits of VCOs shown in Fig. 1(a) and (b). $Z_{in(c)}$ and $Z_{in(p)}$ represent the input impedances of half circuits of conventional and proposed balanced Colpitts VCO, respectively. $R_{n(c)}$, negative resistance of the half circuit of conventional balanced Colpitts-VCO , and $R_{n(p)}$, negative resistance of the half circuit of proposed balanced Colpitts-VCO are calculated from

$$R_{n(c)} = \mathrm{Re}\left[Z_{in(c)} \right] \tag{1}$$

$$R_{n(p)} = \mathrm{Re}\left[Z_{in(p)} \right]. \tag{2}$$

For the oscillation frequency of f_{osc}=3GHz, Fig. 1(d) compares $R_{n(c)}$ and $R_{n(p)}$ that (1) and (2) yield with $Z_{in(c)}$ and $Z_{in(p)}$ obtained from S-parameter simulations using the 0.18 μm RF CMOS technology.

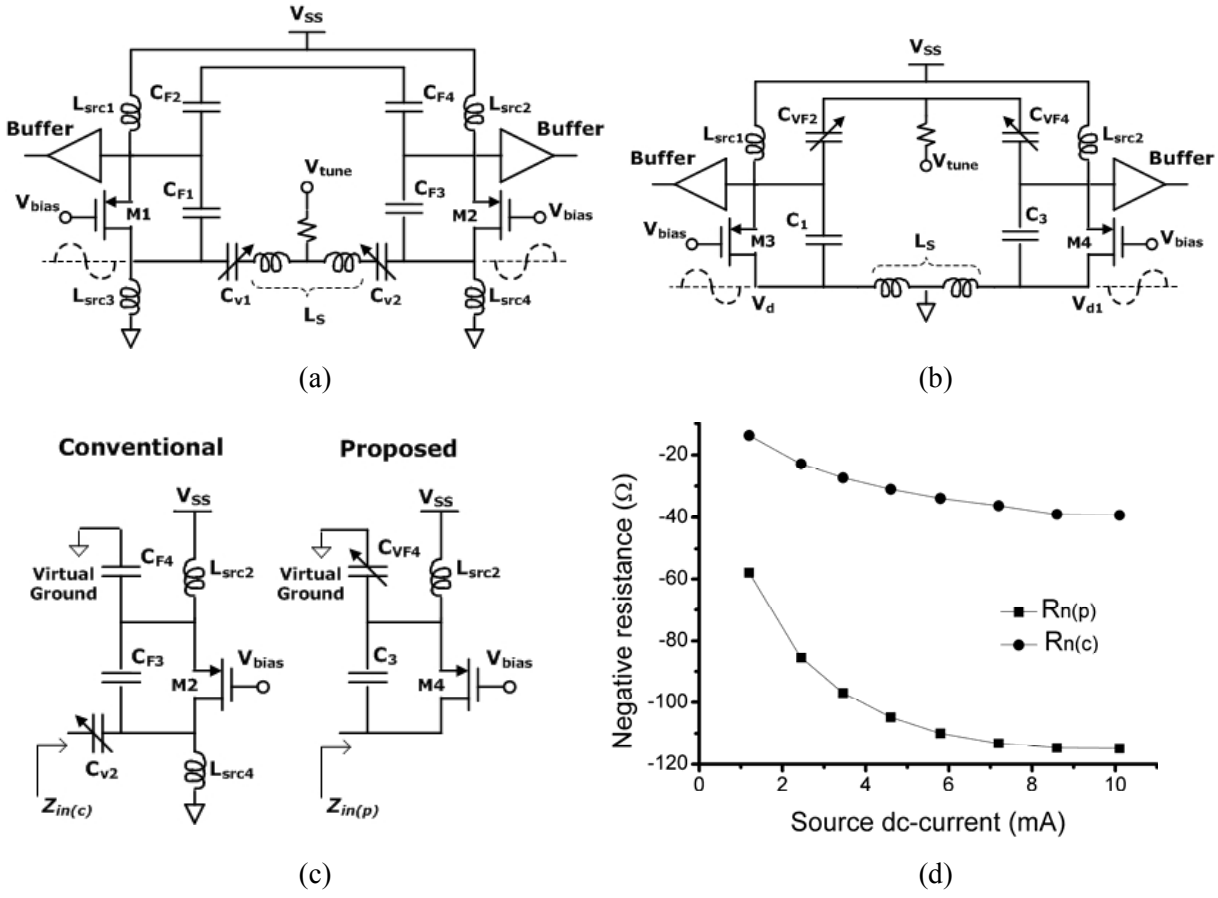


Fig. 1. (a) Conventional balanced Colpitts-VCO employing inductor current sources (b) Proposed balanced Colpitts-VCO (c) Half circuits of conventional and proposed VCO (d) Comparison of negative resistances of half circuits of conventional and proposed VCO.

We can observe that $R_{n(p)}$ vs. source dc-current I_S exhibits much larger negative resistance values than $R_{n(c)}$ *vs.* I_S. This is attributed to the fact that, at the condition of $C_{eq(c)} = C_{eq(p)}$ imposed by the constraint of same oscillation frequency for comparison, capacitances of C_3 and C_{VF4} are usually smaller than those of their corresponding capacitors C_{F3} and C_{F4}. $C_{eq(c)}$ represents the input capacitance of the half circuit of the conventional VCO as shown in Fig. 1(c); $C_{eq(p)}$ the input capacitance of the half circuit of the proposed VCO in Fig. 1(c). $C_{eq(c)}$ and $C_{eq(p)}$ are calculated by following (3) and (4):

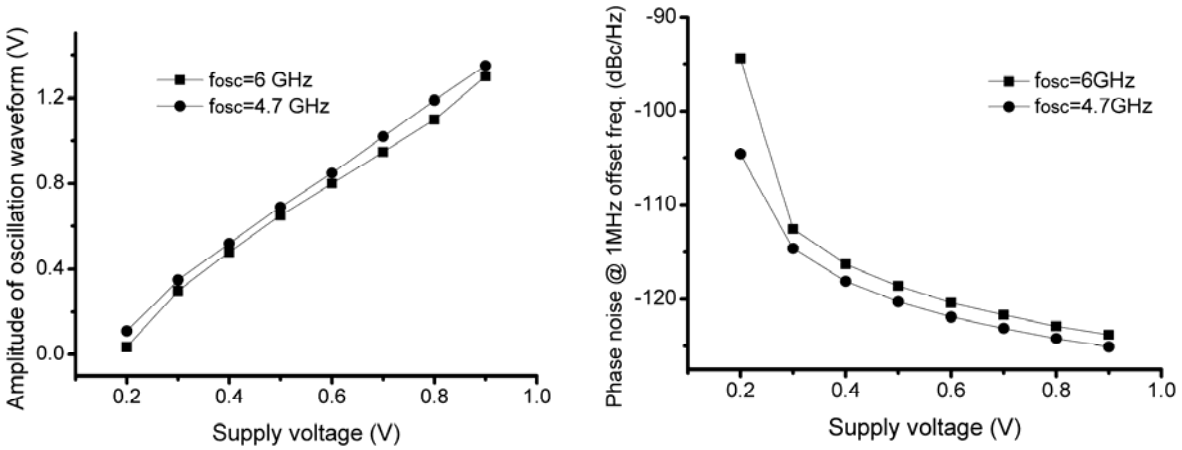
$$C_{eq(c)} = -\left(\omega \mathrm{Im}\left[Z_{in(c)}\right]\right)^{-1} \quad (3)$$

$$C_{eq(p)} = -\left(\omega \mathrm{Im}\left[Z_{in(p)}\right]\right)^{-1}. \quad (4)$$

For comparison of $R_{n(c)}$ and $R_{n(p)}$ at the same oscillation frequency for a given tank inductance, the values of C_{V2}, C_{F3}, C_{F4}, C_3, and C_{VF4} are adjusted so that $C_{eq(c)}$ resulting from C_{V2}, C_{F3}, C_{F4}, and parasitic capacitances of M2 is nearly equal to $C_{eq(p)}$ which decided from C_3, C_{VF4}, and parasitic capacitances of M4. For valid comparison of $R_{n(c)}$ and $R_{n(p)}$, C_{V2} has been set to be equal to C_{VF4}. For the frequencies other than 3GHz, we observed similar behaviors of negative resistances to the case of 3 GHz. It should be noted that the proposed VCO uses PMOSFETs to lower phase noise due to Flicker noise.

3. Simulation Results of the Proposed VCO

Figure 2(a) compares the amplitudes of oscillation waveforms at the V_d and V_{d1} for f_{osc}=4.7 and 6 GHz at the sub-1-V supply voltages. We can observe that the oscillation amplitude for f_{osc}=4.7 GHz is slightly larger than that for f_{osc}=6 GHz, and both of the oscillation amplitudes increase in proportion to the sub-1-V supply voltages. It is noteworthy that, for both of f_{osc}=4.7 and 6 GHz, the amplitudes of oscillation waveforms are always greater than the supply voltage. This is attributed to the tapped structure of capacitors of the tank as shown in Fig. 1(b). The phase noises vs. the sub-1-V supply voltages for two frequencies of f_{osc}=4.7 and 6 GHz are plotted in Fig. 1(b). We can notice that, except for the supply voltage V_{ss}=0.2 V, the phase noises at 1 MHz offset frequency from f_{osc}=4.7 GHz are about 1.5 dBc/Hz lower than that from f_{osc}=6 GHz. We can



(a) (b)

Fig. 2. Post-layout simulation results a 0.18 μm RF CMOS technology: (a) Amplitude of the oscillation waveforms vs. sub-1-V supply voltage (b) Phase noises vs. sub-1-V supply voltage.

also observe that the phase noises decreases as the supply voltage increases. This is attributed to the fact that the amplitude of oscillation signal grows in proportion to the supply voltage V_{ss} as shown in Fig. 2(a). For f_{osc}=6 GHz, Fig. 1(b) exhibits the phase noise of -120.4 to -123.8 dBc/Hz vs. the supply voltages of 0.6 through 0.9 V. It should be noted that the gate bias voltage V_{bias} in Fig. 1(b) is maintained at 0.7 V lower voltage than the sub-1-V supply voltage V_{ss} in order to ensure the stable start-up of oscillation.

The performance comparisons of the proposed VCO and other previously reported VCOs are summarized in Table I. Considering the 0.18 μm technology used in this study, we know that the

phase noise and FOM (Figure of Merit) of the proposed VCO for V_{ss}=0.7 V are comparable to other previously reported VCOs operating at sub-1-V supply voltages.

Table 1: Performance Comparisons with Previous Reports

	[1]	[6]	[7]	[8] (sim.)	This (sim.)
Tech. (μm)	0.13	0.09	0.13	0.13	0.18
Freq. (GHz)	4.9	3.55	3.58	5.2	6
Supply Voltage(V)	0.4	0.22	0.3	0.5	0.7
PN (dBc/Hz)	-132.6 @ 3MHz	-112.97 @ 1MHz	-116.88 @ 1MHz	-117 @ 1MHz	-121.7 @ 1MHz
P_{DC} (mW)	1.92	0.33	0.225	2	4.9
FOM (dBc/Hz)	-193.9	-188.79	-194.43	-188	-190.4
Tuning Range (%)	2.5	5.1	20.4	11.2	7.8

4. Conclusion

The proposed balanced Colpitts-VCO built by applying inductor current sources to the conventional balanced Colpitts VCO with series-tuned tank is suitable for low phase noise oscillation at sub-1-V supply voltages. Additionally, half circuits of the proposed VCO integrate their varactor into one of two feedback capacitors in their respective circuit. This integration makes the negative resistance of the proposed VCO much larger than that of the conventional VCO with series-tuned tank thereby ensuring stable start-up of oscillation even at the sub-1-V supply voltage. When considering that the CMOS technology used in this study has the 0.18 μm gate length, the phase noise and FOM (Figure of Merit) of the proposed VCO for V_{ss}=0.7 V are comparable to those of other previously reported VCOs operating at sub-1V supply voltages.

References

[1] F. Farhabakhshian, T. Brown, K. Mayaram, and T. Fiez, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO in 130 nm CMOS with an FOM of 192.6 dBc/Hz," in *Proc. IEEE CICC 2010*, San Jose, CA, USA, pp. 1-4, Sept. 19-22 2010.

[2] F. Yamashita, T. Matsuoka, T. Kihara, I. Takobe, H.-J. Park, and K. Taniguchi, "Analytical design of a 0.5 V 5 GHz CMOS LC-VCO," *IEICE Electronics Express*, vol. 6, no. 14, pp. 1025-1031, July 2009.

[3] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *IEEE J. Solid-State Circuits*, vol. SC-35, no. 3, pp. 326-336, Mar. 2000.

[4] M.-Y. Jeon, "Differential Clapp voltage controlled oscillator using Metal Oxide Field Effect Transistors," Korea Patent 10-0791169, Dec. 2007.

[5] X. Lee, S. Shekar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. SC-40, no. 12, pp. 2609-2619, Dec. 2005.

[6] S.-L. Jang, C.-J. Huang, C.-C. Liu, and C.-W. Hsue, "A 0.22 V quadrature VCO in 90 nm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol.19, no. 9, pp. 566-568, Sep. 2009

[7] S.-L. Jang, C.-J. Huang, C.-W. Hsue, and C.-W. chang, "A 0.3 V cross-coupled VCO using dynamic threshold MOSFET," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 3, pp. 166-168, Mar. 2010.

[8] B. Catli and M. M. Hella, "A 0.5-V 3.6/5.2 GHz CMOS multi-band LC VCO for ultra low-voltage wireless applications," in *Proc. IEEE ISCAS 2008*, Seattle, WA, USA, May 18-21 2008, pp. 996-999.