A 24GHz CMOS RF Transceiver for Car Radar Applications

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Abstract

This paper describes a 24GHz CMOS RF transceiver for car radar applications. The transceiver consists of 4-channel receiver array and 1-channel transmitter. The prototype is designed by standard RF CMOS 0.13-μm technology. The simulated receiver gain is 30dB and simulated tramsmitted output power is 15dBm at 24GHz.
Keywords : CMOS RF Transceiver Car radar

1. Introduction

Until now, automotive radar products in K-band have been developed in GaAs technologies because of the excellent performance of the technologies [1]-[2]. However the fabrication cost of GaAs technologies is too high to make it commonly used feature. CMOS technology has merits of a higher level of integration and lower cost than the III-V compounds, enabling the production of multifunction RF transceivers and RF system-on-chip designs. Therefore, the research and development of silicon-based solutions for millimetre-wave applications have gained significant momentum in recent years.

As one of ISM bands, 24-GHz has versatile application including short and mid range automotive radar. Especially, frequency modulated continuous wave (FMCW) radar has been adopted widely due to its simplicity. This paper describes a 24-GHz CMOS RF transceiver with 4-receiver arrays for middle radar range car applications. The proposed transceiver consists of 4-channel receiver array, 1-channel transmitter, 24GHz frequency generator with phase locked loop and 24GHz CMOS power amplifier (PA). Also, two bandgap circuits, low drop-out regulators and a temperature sensor help this system stabilize over wide temperature operating range. The block diagram of the proposed RF transceiver is shown in Fig. 1.

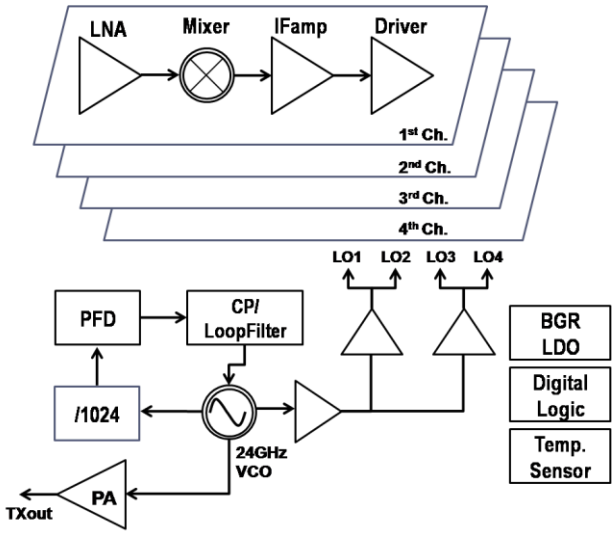


Figure 1: Block diagram of the proposed 24GHz CMOS transceiver.

2. RF Transceiver System Design

2.1 **Overall Architecture**

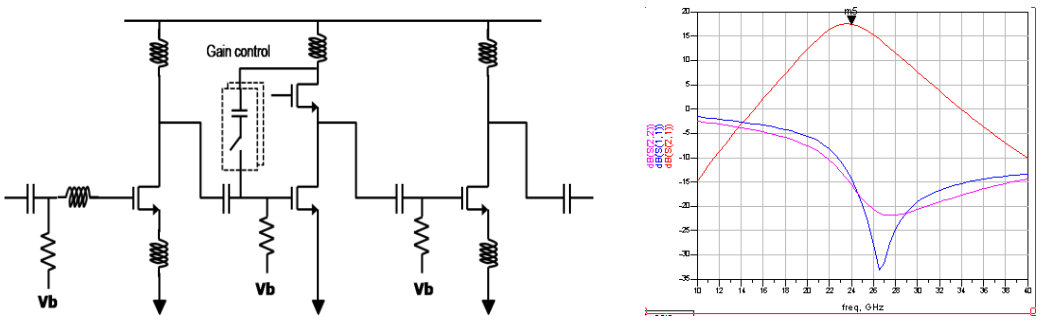
In FMCW radar system, detection range and minimum detectable distance depend on the receiver's noise figure and phase noise of voltage controlled oscillator (VCO). Also, the linearity of the receiver should be guaranteed to distinguish the reflected our signal under various incoming interference signal. Also, when array system is adopted to increase detection range, phase alignment is very critical. Thus, we utilized digital beam forming technique, which can simplify transceiver design. In the receiver design, only four receiver chains are used repeatedly with one local oscillator (LO). Also, same LO block is reused for transmitting RF signal due to synchronize FMCW.

2.2 **Receiver Design**

In the receiving front, low noise amplifier (LNA) has a role of deciding overall receiver's noise figure. Therefore, the noise and power matching should be obtained simultaneously [3]. In standard 0.13-μm CMOS technology, the RF transistor was simulated over gate voltage in terms of maximum achievable gain (MAG). Without sacrificing linearity of LNA, the LNA adopts three stage using degeneration inductors as shown in Fig. 2. In the first and third stages, degenerated inductors are used for noise matching and high linearity. In the second stage, the degenerated inductor did not adopt to increase power gain. Overall simulated results were S21 of 18dB, NF of 4dB and IIP3 of -6.6dBm. For mixer design, low NF is critical to detect close object in FMCW modulation. Generally, passive mixer has lower NF characteristic than active mixer. Although passive mixer requires high amplitude swing LO signal, the large swing can be obtain by extra LO buffer stage in terms of current consumption, which is not a burden in car application. Backend baseband stage consists of ADC driver and gain amplifier to reduce ADC specification burden.

2.3 **Transmitter Design**

In the transmitting part, VCO output signal is fed to an integrated PA. Therefore, to accomplish single-chip radar, a CMOS PA is integrated in the transceiver. To minimize interaction between PA and other working blocks such as PLL, an individual LDO is used to block power/ground coupling due to the large current flows. Fig. 3 shows the schematic of the designed PA. PA consists of two-stage to ensure enough power gain due to small input signal from an internal power mismatching [4]. Also, 50Ω output matching is obtained by internal integrated balun. The simulated PA performances showed that power gain of 23dB, P_{-1dB} of 13dBm, P_{sat} of 15.3dBm and power-added efficiency of 15.2%.



(a) (b)

Figure 2: LNA (a) schematic and (b) simulated results

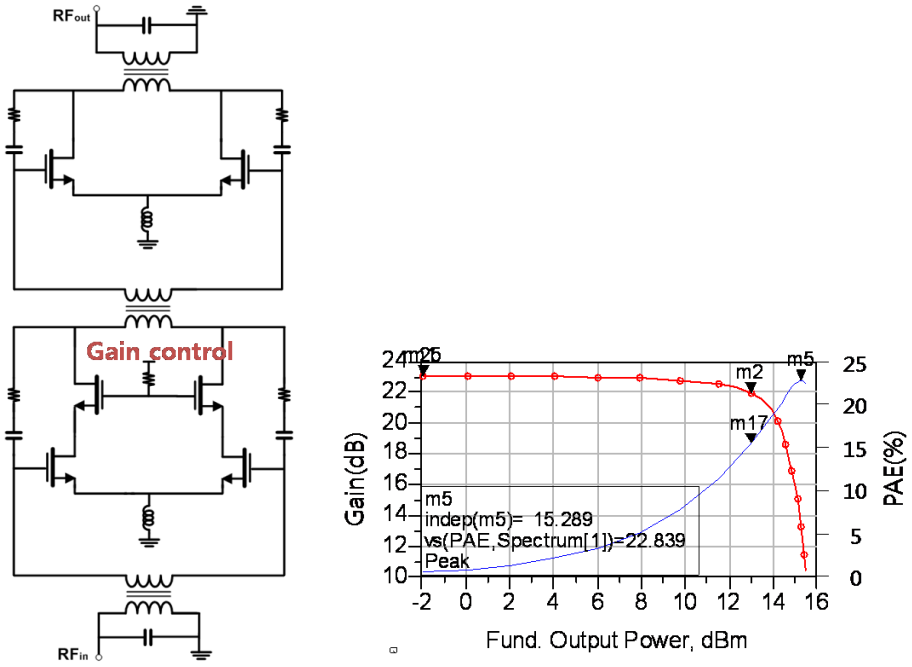


Figure 3: CMOS 24GHz PA (a) schematic and (b) simulated results

2.3 **PLL Design**

In the FMCW modulation, signal generator is a one of key blocks, because VCO signal decide down-converted signal's quality. An LC cross-coupled VCO with NMOS pairs was adopted to guarantee stable operation. Integrated charge pump and loop filter have controllable resistors and capacitors, which can be post-tuned for the optimized PLL bandwidth by digital logics such as SPI. Also, power supply was separated between charge pump block and VCO, divider and loop filter to prevent interaction, reducing unwanted spurious tones. Frequency divider is one of challenging block in 24GHz PLL. In this design, divider-1024 was designed using cascaded divder-2 cells. Generally, injection locked divider has small operating frequency range. Thus, a miller divider was adopted in the first divider-2 cell to ensure fast and stable operation [5]. In the second and third divider-2, CML-type divider was used for small area. In the rest dividers, dynamic TSPCs and static flipflops are employed.

2.4 **Chip Layout**

Overall CMOS transceiver is fabricated in standard 0.13-μm CMOS technology. Fig. 4 shows the layout photograph. The overall layout size is 2.5mm × 2.5mm. In the left side, 4-array receiver chains are placed with LDO. In the right side, PLL circuitry and temperature sensor are placed to isolate from the receiver array. The PA is located at the bottom of right side with individual power and ground pads. The LO signal routing is evenly divided into mixers of receiver array to prevent LO signal mismatch. This chip is now under fabrication

3. Summary

In this paper, a 24-GHz CMOS RF transceiver is proposed. In the transceiver, power amplifier is integrated to achieve single-chip radar solution. Also, integrated LDOs and temperature sensor help this chip achieve stable operation over wide temperature variations. The simulated results show that NF and IIP3 of receiver are 6dB and -12dBm and 13dBm transmitting RF output power. Based on these design and performance, this solution can fertilize CMOS-based radar single-chip.

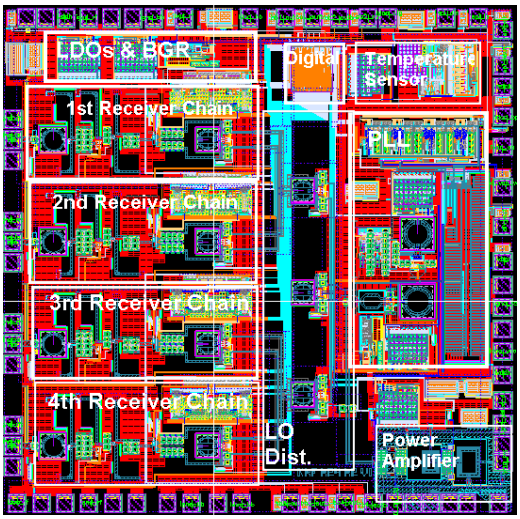


Figure 4: Layout photograph of the proposed 24GHz CMOS transceiver.

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Acknowledgments

This work was supported by the System IC 2010 Project (10030846, Development of Radar and Image Based High Safety SoC for Automotive) funded by the Ministry of Knowledge Economy (MKE), Korea.