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Biobjective Optimization Problems in Paralleled Boost Converters

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Abstract—This paper studies a biobjective optimization problem in a paralleled boost converters which are widely used in renewable energy supply systems. In order to define the biobjective optimization problem, we define two objectives for circuit stability and power efficiency. Using piecewise linear modeling, the two objectives and the Pareto front are obtained exactly. The Pareto front guarantees existance of a trade-off between the two objectives.Presenting a simple circuit, typical circuit operations are confirmed experimentally.

1. Introduction

The multiobjective optimization problems (MOPs) are inevitable and important in various fields of natural science including power electronics. The MOPs require simultaneous optimization of multiple objectives where we often encounter various difficulties such as the presence of conflicting objectives. An improvement in one objective may cause a deterioration in another objective. In such cases, an important task is to find a Pareto front in the objective space that describes the best trade-off. In order to find the Pareto front, efficient evolutionary algorithms have been presented and have been applied to bench mark problems [1] [2]. In various engineering systems, a system performance is evaluated by multiple objectives. However, MOPs in concrete engineering systems have not been studied sufficiently.

This paper studies a biobjective optimization problem (BOP, the simplest MOP) in a paralleled boost converters. The paralleled systems are suitable to realize ripple reduction and current sharing for reliable and efficient renewable energy supply [3]. The boost converters are widely used in renewable energy systems [4]. For simplicity, we introduce a piecewise linear (PWL) model of the circuit where the dynamics can be analyze exactry [5] [6].

First, we define two objectives. The first objective evaluates circuit stability and the second objective evaluates input power efficiency. In the piecewise linear model, the two objectives described exactly and precise analysis is possible. Using the two objectives, we defines the BOP. After simple theoretical calculation, we obtain the Pareto front between the two objectives. The Pareto front is derived exactly and guatantees existence of a trade-off between the two objectives. Presenting a simple test circuit, typical circuit operations are confirmed experimentally. These rusults gives important basic information to design efficient power converters.

2. Piecewise Linear Circuit Model

Fig. 1 shows PWL circuit model of paralleled boost converters. The circuit extracts input power. V_{in} corresponds to input and V_{out} corresponds to output load. The switch S_j and the diode D_j ($j = 1$ or 2) can be either of the four states:

State A_1: S_1=on, D_1=off
State B_1: S_1=off, D_1=on
State A_2: S_2=on, D_2=off
State B_2: S_2=off, D_2=on

The circuit dynamics is described by

$$L_1\frac{di_1}{dt} = \begin{cases} V_{in} & \text{State } A_1 \\ V_{in} - V_{out} & \text{State } B_1 \end{cases}$$
$$L_2\frac{di_2}{dt} = \begin{cases} V_{in} & \text{State } A_2 \\ V_{in} - V_{out} & \text{State } B_2 \end{cases} \quad (1)$$

where $V_{out} > V_{in}$ in the boost operation.

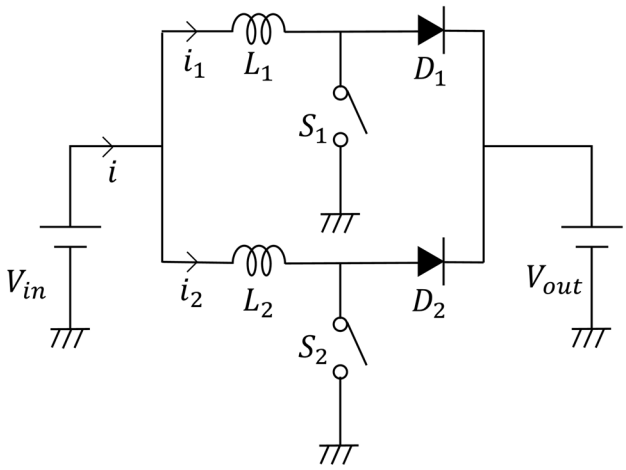

Figure 1: Circuit model

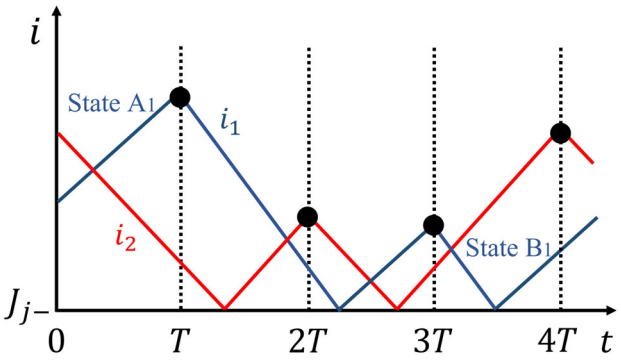

Figure 2: Switching rule

The switching rules are defined by

$$\begin{cases} \text{State A}_1 \to \text{State B}_1 \text{ when } i_1 > i_2 \text{ at } t = nT \\ \text{State B}_1 \to \text{State A}_1 \text{ if } i_1 = J_{1-} \end{cases}$$

$$\begin{cases} \text{State A}_2 \to \text{State B}_2 \text{ when } i_2 > i_1 \text{ at } t = nT \\ \text{State B}_2 \to \text{State A}_2 \text{ if } i_2 = J_{2-} \end{cases}$$

where J_{1-} and J_{2-} are the lower thresholds for i_1 (respectively, i_2). T is period of the clock signal. Fig. 2 illustrates switching rules.

For simplicity, we assume that the time constant RC of the output load is larger than the clock period T. In this case, we can simplify the RC load into a constant voltage source V_{out}. Using the following dimensionless variables and parameters

$$\tau = \frac{t}{T},\ x_1 = \frac{i_1 - J_{1-}}{I_p - J_{1-}},\ x_2 = \frac{i_2 - J_{2-}}{I_p - J_{2-}},$$

$$a_1 = \frac{T}{L_1(I_p - J_{1-})} V_{in},\ b_1 = \frac{T}{L_1(I_p - J_{1-})}(V_{out} - V_{in}),$$
$$a_2 = \frac{T}{L_2(I_p - J_{2-})} V_{in},\ b_2 = \frac{T}{L_2(I_p - J_{2-})}(V_{out} - V_{in})$$

Eq. (1) is transformed into

$$\frac{dx_1}{d\tau} = \begin{cases} a_1 & \text{State A}_1 \\ -b_1 & \text{State B}_1 \end{cases}$$
$$\frac{dx_2}{d\tau} = \begin{cases} a_2 & \text{State A}_2 \\ -b_2 & \text{State B}_2 \end{cases} \qquad (2)$$

Switching rule

$$\begin{cases} \text{State A}_1 \to \text{State B}_1 \text{ when } x_1 > x_2 \text{ at } \tau = n \\ \text{State B}_1 \to \text{State A}_1 \text{ if } x_1 = 0 \end{cases}$$

$$\begin{cases} \text{State A}_2 \to \text{State B}_2 \text{ when } x_2 > x_1 \text{ at } \tau = n \\ \text{State B}_2 \to \text{State A}_2 \text{ if } x_2 = 0 \end{cases}$$

Using the exact piecewise solutions, we can calculate wave forms exactly. Fig. 3 shows typical examples of two phase synchronized periodic waveforms with period 2; (a) a waveform with weak stability and small ripple, (c) a waveform with strong stability and large ripple, (b) a waveform with characteristics between (a) and (c). Fig. 3 suggests that there is a trade-off between stability and ripple. We will discuss this in the next section.

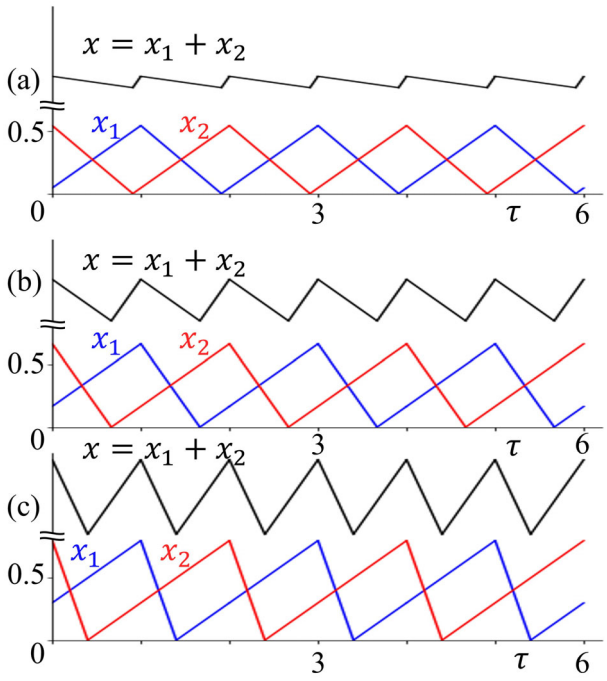

Figure 3: Waveform examples. $a = 0.50$, (a) $b = 0.60$, $|Df(p)| = 0.83$, $Y = 0.09$, (b) $b = 1.00$, $|Df(p)| = 0.50$, $Y = 0.33$, (c) $b = 2.00$, $|Df(p)| = 0.25$, $Y = 0.60$, $|Df(p)|$ is parameter ratio a/b, and Y is ripple of x

In order to confirm the waveforms in laboratory, we have designed a hardware prototype as shown in Fig. 4. The inductor current waveform was measured using a current-to-voltage converter (IVC).

We have confirmed 2-phase synchronization waveforms as shown in Fig. 5; (a) a waveform with weak stability and small ripple, (c) a waveform with strong stability and large ripple, (b) a waveform with characteristics between (a) and (c). In this experiment,we can see that there is a trade-off between stability and ripple.

3. Biobjective Optimization Problems

In this paper, we focus on stable 2-phase synchronization waveforms. In order to evaluate stability of periodic orbit period 2, we introduce contraction rate $|Df(p)| \equiv |\frac{\Delta x(2)}{\Delta x(0)}|$ near the orbit as show in Fig. 6. p is an initial point of the two-phase synchronized periodic waveforms with period 2 ($x_1(0) = p, x_1(0) = x_1(2) = p, x_2(1) = x_2(3) = p$).

In order to define the BOP, we define two objectives

$$F_1(a,b) = |Df(p)| = |\frac{\Delta x(2)}{\Delta x(0)}| = \frac{a}{b} \equiv X$$
$$F_2(a,b) = (1 - \frac{a}{b})\frac{2ab}{a+b} \equiv Y \qquad (3)$$

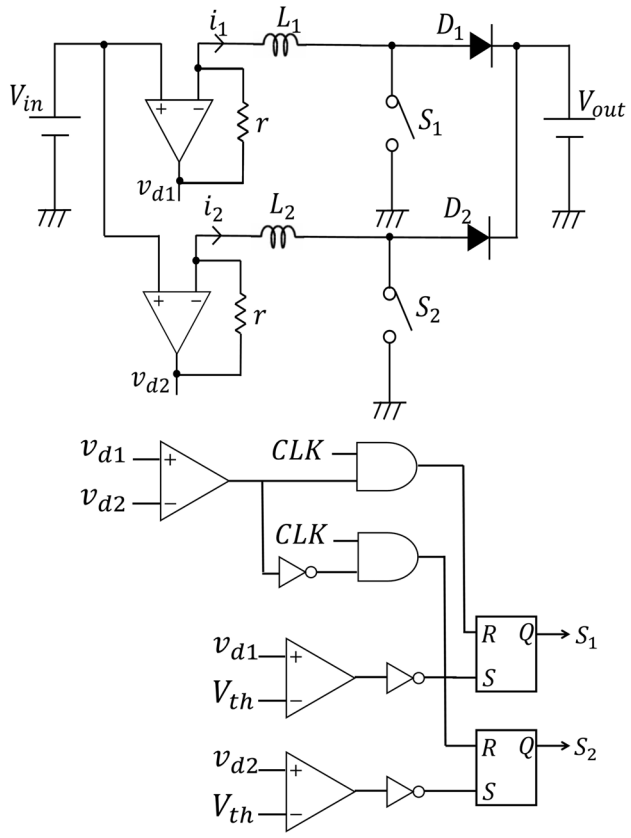

Figure 4: Hardware prototype

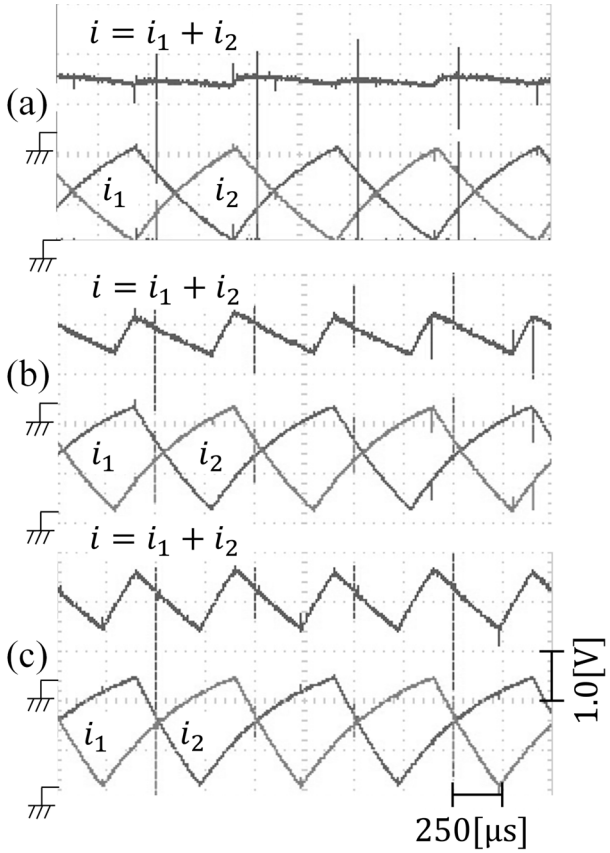

Figure 5: Measured waveforms. $T \doteq 0.50$[ms], $L_1 = L_2 \doteq 100$[mH], $V_{in} \doteq 1.15$[V], $V_{th} \doteq 1.20$[V], and $r \doteq 1.0$[kΩ] (a) $V_{out} \doteq 1.20$[V], $a/b \doteq 0.91$, (b) $V_{out} \doteq 1.50$[V], $a/b \doteq 0.60$, (c) $V_{out} \doteq 1.70$[V], $a/b \doteq 0.48$.

where $a_1 = a_2 \equiv a$, $b_1 = b_2 \equiv b$, and $a = 0.5$ to simplify the analysis. F_1 is objective of stability. The F_1 approaches zero, the stronger the stability. F_2 is objective of ripple of paralleled converters The F_2 approaches zero, the more efficient the circuit. It should be noted that the two objective functions can be calculated precisely using the exact piecewise solutions.

We define biobjective optimization problem.

$$\begin{aligned} &\text{Minimize } F(a,b) = (F_1(a,b), F_2(a,b)) \\ &\text{subject to } (a,b) \in \{(a,b) | a = 0.5, a < b < 100\} \end{aligned} \tag{4}$$

The Pareto front between stability and ripple can be calculated precisely as follows.

$$Y = 2a\tfrac{1-X}{1+X},\ 0 < X < 1 \tag{5}$$

Fig. 7 shows Pareto front between stability and ripple. where the horizontal axis represents the stability and the vertical axis represents the ripple.

4. Conclusions

A BOP in paralleled boost converters has been studied in this paper. Using the piecewise linear modeling, the Pareto front is obtained exactly. It guaranteed existance of a trade-off between circuit stability and input power efficiency. In our future work, we should consider more detailed analysis of the BPOs in boost converters with photovoltaic input.

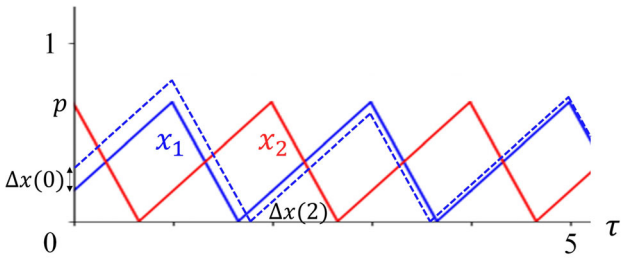

Figure 6: Stability

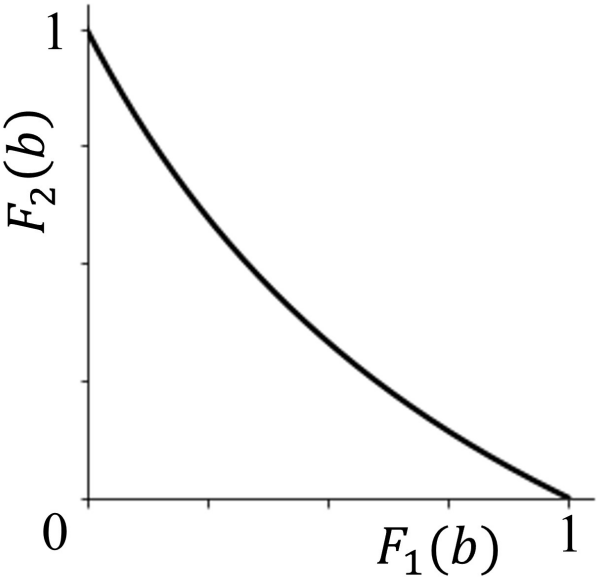

Figure 7: Pareto front($a = 0.50$)

References

[1] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, A fast and elitist multiobjective genetic algorithm: NSGA-II IEEE Trans. Evol. Comput. 6, 2, pp. 182-197, 2002.

[2] Q. Zhang and L. Hui, MOEA/D: A multiobjective evolutionary algorithm based on decomposition, IEEE Trans. Evol. Comput., 11, 6, pp. 712-731, 2007.

[3] R. Giral and L. Murtinez-Salamero, Interleaved converters operation based on CMC, IEEE Trans. Power Electron., 14, 4, pp. 643-652, 1999.

[4] S. Selvakumar, M. Madhusmita, C. Koodalsamy, S. P. Simon and Y. R. Sood, High-speed maximum power point tracking module for PV systems, IEEE Trans. Ind. Electron, 66, 2, pp. 1119-1129, 2019.

[5] T. Togawa, Y. Kunii, S. Yasukawa and T. Saito, Application of MOEA/D to a trade-off problem between maximum power point and stability, Proc. IEEE/CEC, 2019.

[6] T. Saito and D. Kimura, Synchronization and hyperchaos in switched dynamical systems based on parallel buck converters, IEICE Trans. Fundamentals, E92-A, 8, pp. 2061-2066, 2009.