2009 International Symposium on Nonlinear Theory and its Applications
NOLTA'09, Sapporo, Japan, October 18-21, 2009

Analysis of Paralleled Switched-Capacitor DC-DC Converters with Voltage-Controlled Switching

Hiroyuki Nakamura† and Toshimichi Saito†

†EE Dept., Hosei University, Koganei, Tokyo, 184-0002 Japan; tsaito AT hosei.ac.jp

Abstract—This paper presents a novel switched-capacitor dc-dc converters consisting of two sub-circuits connected in parallel. Switches in the circuit are controlled not only by periodic clock signal but also by a capacitor voltage. The voltage-controlled switching is a key to realize stable and variable output with fast transient. The circuit dynamics is described by piecewise linear equation and can be integrated into a 1-D return map: we can analyze the system dynamics precisely. Especially, it is clarified theoretically that the SC converter can realize superstable steady state with extremely fast transient.

1. Introduction

Switched-capacitor (SC) technology has been used widely in low-power dc-dc converters and have been improved to meet power management of future integrated circuits [1] [2]. It is estimated that the supply voltage for future microprocessors will decrease from 3.5 to 1 V and even lower, in order to decrease the power loss of modern high power consumption CPUs. In order to realize such a power supply, there are many requirements including the following three points: (1) Fast transient to steady state, (2) Variable output voltage in a desired range, (3) lower voltage with higher current capability for highly integrated circuits [3] [4].

In order to consider these requirements, this paper presents a novel SC dc-dc converter and analyze the operation. The converter consists of two sub-circuits connecting in parallel. Each sub-circuit includes several switches each of which is controlled not only by periodic clock signal but also by a capacitor voltage. The voltage-controlled switching is a key to realize stable and variable output with fast transient. The parallel operation is basic for current sharing that is a key to meet higher current capability and to realize output ripple reduction [3]. The circuit dynamics is described by piecewise linear equation [5] and can be integrated into a 1-D return map formulated explicitly. The piecewise exact solution and return map enable us to analyze transient dynamics and system stability precisely. As a remarkable results, it is clarified theoretically that the SC converter can realize superstable steady state with extremely fast transient. Typical circuit operations are confirmed in numerical simulation.

It should be noted that steady state analysis has been mainstream in existing works on SC converters [6]. Transient and stability have not been analyzed sufficient so far. This paper can be a trigger to design efficient SC converters and to develop precise analysis method of stability and transient characteristics.

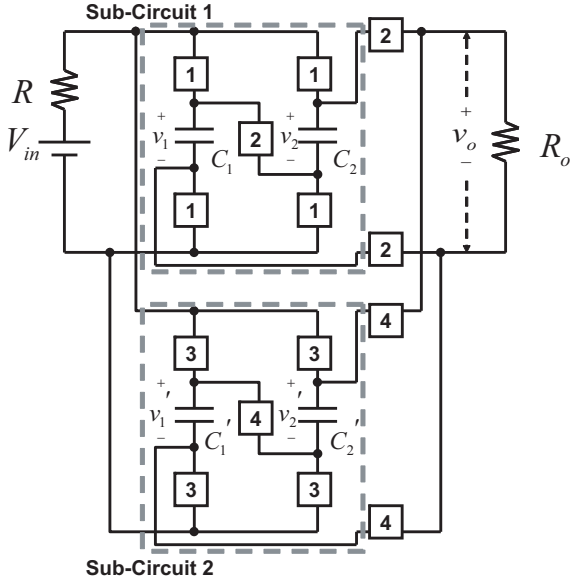

Figure 1: Paralleled Switched-Capacitor Boost Converters

2. Paralleled Converters

Fig. 1 shows the paralleled switched-capacitor boost converter. The input is converted to the output through two sub-circuits which includes controlling switches 1 to 4. The sub-circuit 1 can be either of the following three states:

State 1: S_1=ON, S_2=OFF
State 2: S_1=OFF, S_2=ON
State 3: S_1=OFF, S_2=OFF

The sub-circuit 2 can be either of the following three states:

State 4: S_3=ON, S_4=OFF
State 5: S_3=OFF, S_4=ON
State 6: S_3=OFF, S_4=OFF

Transition among these states depends on clock signal with period T and the capacitor voltage v_1 and v_2 as shown in Fig. 2. The switching rule for the sub-circuit 1 is defined by

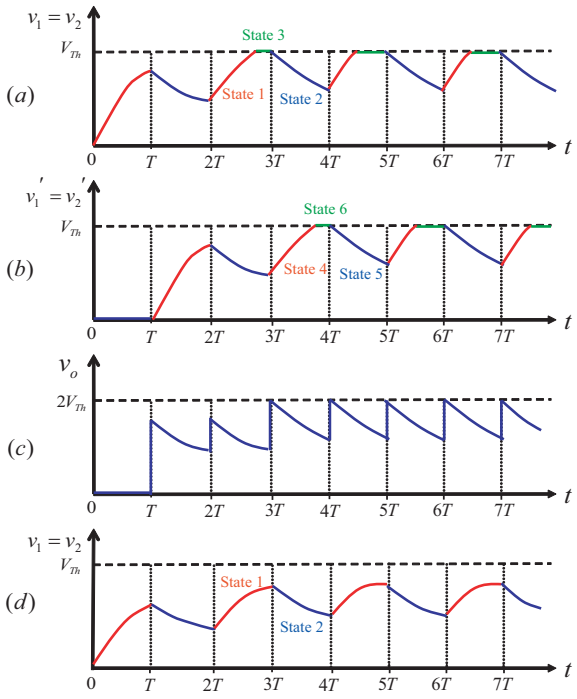

Figure 2: Switching rule and voltage waveforms for $v_1(0)$=$v_2(0)$ and $v_1'(0)$=$v_2'(0)$.

$$\begin{aligned} &\text{State 1} \rightarrow \text{State 3 if } v_1 = V_{Th} \\ &\text{State 1 or 3} \rightarrow \text{State 2 if } t = (2n-1)T \\ &\text{State 2} \rightarrow \text{State 1 if } t = 2nT \end{aligned} \tag{1}$$

where n denotes positive integers. Switches in the sub-circuit 2 has phase shift T for the sub-circuit 1: the switching rule is given by

$$\begin{aligned} &\text{State 4} \rightarrow \text{State 6 if } v_1' = V_{Th} \\ &\text{State 4 or 6} \rightarrow \text{State 5 if } t = 2nT \\ &\text{State 5} \rightarrow \text{State 4 if } t = (2n+1)T \end{aligned} \tag{2}$$

In Fig. 2 (a) to (c) we can see that once the capacitor voltage reach the threshold V_{Th}, the steady state operation can be achieved. $v_1 + v_2$ is supplied to the load in the state 2 and $v_1' + v_2'$ is supplied to the load in the state 5: the two sub-circuits supply the output voltage v_o alternately. If the threshold V_{Th} exceeds a limit value, the capacitor voltage v_1 can not reach the threshold V_{Th}, State 3 can not exist and the steady state operation can not be achieved within finite time in theoretical sense as suggested in Fig. 2 (d). Such circuit behavior is analyzed in the next section.

3. Stability analysis

Here we consider stability and transient properties. The two sub-circuits operates in phase shift T to each other. The dynamics of the sub-circuit 1 is described by the following equation and the switching rule (1):

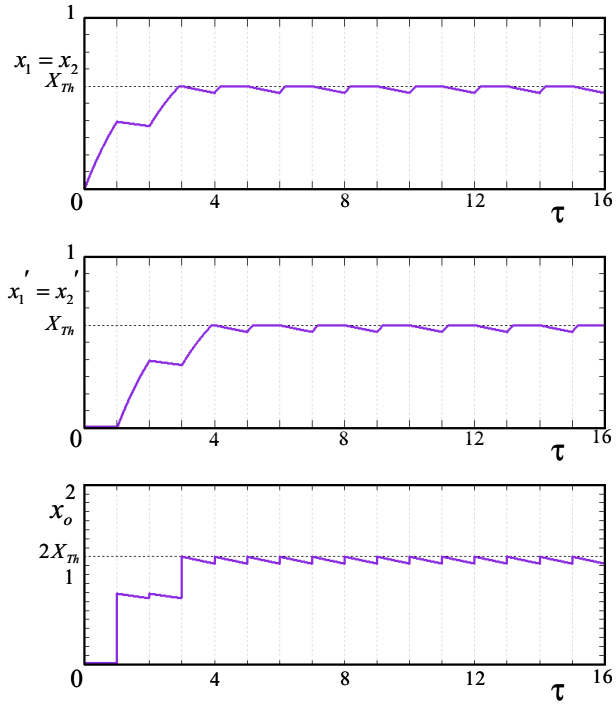

Figure 3: Typical waveforms for (α, β, γ, δ, X_{Th})=(1, 1, 30, 30, 0.6)

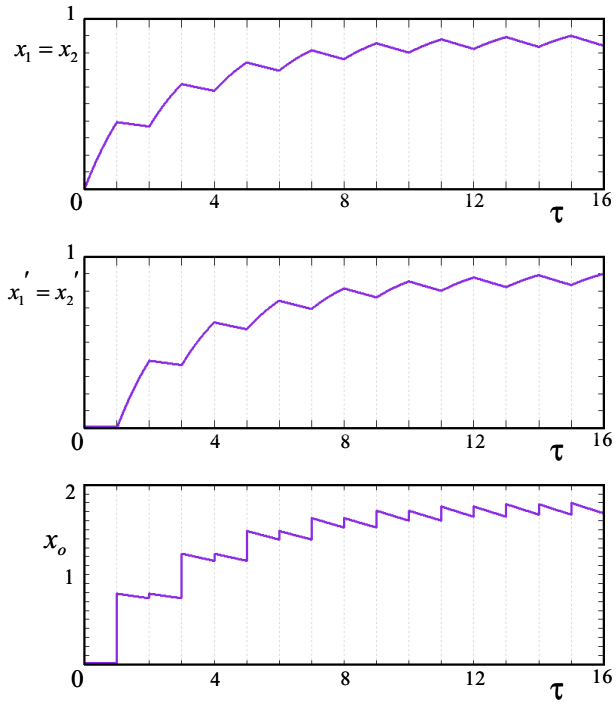

Figure 4: Typical waveforms for (α, β, γ, δ, X_{Th})=(1, 1, 30, 30, 1)

$$\begin{aligned} &\dot{v}_1 = -\frac{1}{RC_1 + RC_2}(v_1 - 1),\ v_1 = v_2 && \text{for State 1} \\ &\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \end{pmatrix} = \begin{pmatrix} -\frac{1}{R_oC_1} & -\frac{1}{R_oC_1} \\ -\frac{1}{R_oC_2} & -\frac{1}{R_oC_2} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} && \text{for State 2} \\ &\dot{v}_1 = 0,\ v_1 = v_2 && \text{for State 3} \end{aligned} \tag{3}$$

Note that $v_1 = v_2$ is satisfied the State 1. We define the following dimensionless variables and parameters:

$$\tau = \frac{t}{T},\ x_1 = \frac{v_1}{E},\ x_2 = \frac{v_2}{E},\ \text{"}\cdot\text{"} \equiv \frac{d}{d\tau},\ X_{Th} = \frac{v_{Th}}{E},$$
$$\alpha = \frac{RC_1}{E},\ \beta = \frac{RC_2}{T},\ \gamma = \frac{R_oC_1}{T},\ \delta = \frac{R_oC_2}{T}$$

Using these, Eq. (3) and switching rule (1) are transformed into

$$\begin{aligned} &\dot{x}_1 = -\frac{1}{\alpha+\beta}(x_1 - 1),\ x_1 = x_2 && \text{for State 1} \\ &\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \end{pmatrix} = \begin{pmatrix} -\gamma^{-1} & -\gamma^{-1} \\ -\delta^{-1} & -\delta^{-1} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} && \text{for State 2} \\ &\dot{x}_1 = 0,\ x_1 = x_2 && \text{for State 3} \end{aligned} \tag{4}$$

State 1 → State 3 if $x_1 = X_{Th}$
State 1 or 3 → State 2 if $\tau = 2n - 1$
State 2 → State 1 if $\tau = 2n$

This is the dimensionless equation for the sub-circuit 1. Repeating in a likewise manner, we obtain the the dimensionless equation for the sub-circuit 2.

$$\begin{aligned} &\dot{x'}_1 = -\frac{1}{\alpha+\beta}(x'_1 - 1),\ x'_1 = x'_2 && \text{for State 4} \\ &\begin{pmatrix} \dot{x'}_1 \\ \dot{x'}_2 \end{pmatrix} = \begin{pmatrix} -\gamma^{-1} & -\gamma^{-1} \\ -\delta^{-1} & -\delta^{-1} \end{pmatrix}\begin{pmatrix} x'_1 \\ x'_2 \end{pmatrix} && \text{for State 5} \\ &\dot{x'}_1 = 0,\ x'_1 = x'_2 && \text{for State 6} \end{aligned} \tag{5}$$

State 4 → State 6 if $x'_1 = X_{Th}$
State 4 or 6 → State 5 if $\tau = 2n$
State 5 → State 4 if $\tau = 2n + 1$

where $x'_1 = v'_1/E$ and $x'_2 = v'_2/E$. Also, we have assumed $C_1 = C'_1$ and $C_2 = C'_2$. Figs. 3 and 4 show typical waveforms corresponding to Fig. 2. They are calculated by piecewise exact solution of Eq. (5). Since $x_1(n)$ determines $x_1(n+2)$, we can define the return map that is useful to analyze stability. Using the exact piecewise solution the map can be expressed explicitly:

$$x_1(n+2) = F(x_1(n))$$
$$F(x_1(n)) = \begin{cases} ax_1(n) + b & \text{for } 0 < x_1(n) < X_D \\ X_{Th} & \text{for } X_D < x_1(n) < 1 \end{cases} \tag{6}$$

where

$$a = \exp(-(\frac{1}{2\alpha} + \frac{2}{\gamma})\tau)$$
$$b = 1 - \exp(-\frac{1}{2\alpha}\tau))$$
$$X_D = \frac{1}{a}(X_{Th} - b).$$

Figs. 5 (a) and (b) show typical shapes of the return map corresponding to Figs. 3 and 4, respectively. Note that the flat branch ($x_1(n) = X_{Th}$) can not exist if $X_D < 0$ as shown in Fig. (b). In Fig. 5 (a), the map has superstable fixed point x_s corresponding to the steady state. The orbit started from $[0, 1)$ can reach the fixed point within a finite time, that is, the steady state can be achieved within a finite time. Such superstable fixed point can exist if

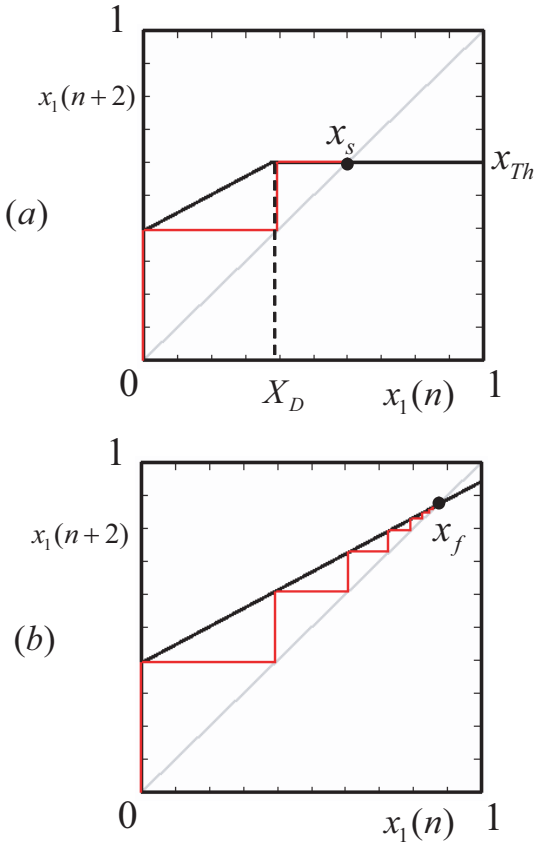

Figure 5: Return maps for (α, β, γ, δ)=(1, 1, 30, 30). (a) X_{Th}=0.6. (b) X_{Th}=1.

$$F(X_D) > X_D \tag{7}$$

Fig. 5 (b) does not has the flat branch and the orbit converges to the stable fixed point x_f: the steady state can not be achieved within finite time. Using the exact piecewise solution, we can calculate the transient time and that for zero initial state $x_1(0) = x_2(0) = 0$ is shown in Fig. 6: as X_{Th} increases, the transient process is to be long and the superstable condition(7) is destroyed.

We have also investigated ripple characteristics as shown in Fig. 7, where the ripple is measured by amplitude of the dimensionless output waveform in the steady state:

$$R_f = |x_{max} - x_{min}| \tag{8}$$

The ripple factor R_f decreases as the parameter $\gamma = \frac{R_oC_1}{T}$ and $\delta = \frac{R_oC_2}{T}$ increases.

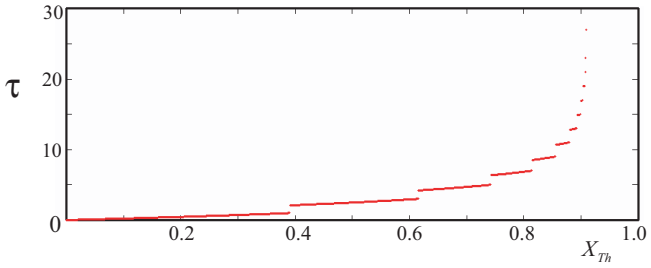

Figure 6: Transition Characteristic. (α, β, γ, δ)=(1, 1, 30, 30).

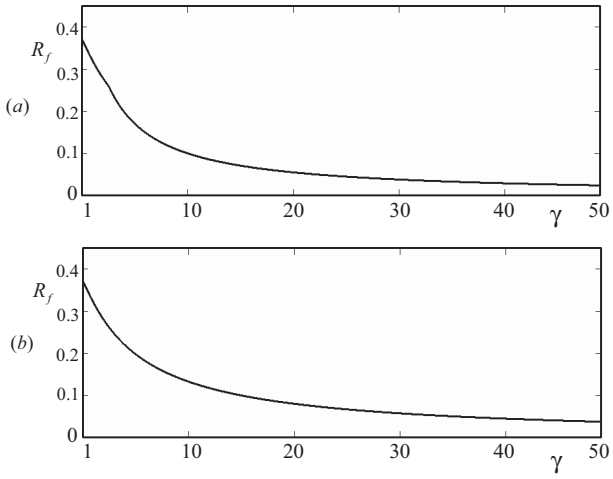

Figure 7: Ripple characteristics for (α=β=1, γ=δ). (a) for X_{Th}= 0.6 and (b) for X_{Th}=1 correspond to Figs. 4 and 5, respectively.

4. Conclusions

We have presented paralleled switched-capacitor DC-DC converter whose switching is controlled by clock signal and threshold voltage V_{Th}. This switching realize super-stable operation of wide range output and the steady state can be achieved within a finite time. The parall operation is suitable for lower-voltage higher-current capability with lower output ripple. Future problems include application of various switching rules, more detailed analysis of stability for initial state and parameters, and design of practical circuits.

References

[1] B. Axelrod, Y. Berkovich and A. Ioinovici, Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC-DC PWM Converters, IEEE Trans. Circuits Systs. I, 55, 2, pp. 687-696, 2008

[2] F. Zhang, L. Du, F. Z. Peng and Z. Qian, A New Design Method for High-Power High-Efficiency Switched-Capacitor DC-DC Converters, IEEE Trans. Power Electron., 23, 2, pp. 832-840, 2008

[3] R. Giral and L. Murtinez-Salamero, Interleaved converters operation based on CMC, IEEE Trans. Power Electron., 14, 4, pp. 643-652, 1999

[4] X. Zhou, P. Xu and F. C. Lee, A novel current-sharing control technique for low-voltage high-current voltage regulator module applications, IEEE Trans. Power Electron., 15, 6, pp. 1153-1162, 2000.

[5] T. Saito, T. Kabe, Y. Ishikawa, Y. Matsuoka and H. Torikai, Piecewise constant switched dynamical systems in power electronics, Int'l J. of Bifurcation and Chaos, 17, 10, pp. 3373-3386, 2007.

[6] M. D. Seeman and S. R. Sanders, Analysis and Optimization of Switched-Capacitor DC-DC Converters, IEEE Trans. Power Electron., 23, 2, pp. 841-851, 2008

[7] T. Saito, S. Tasaki and H. Torikai, Interleaved buck converters based on winner-take-all switching, IEEE Trans. Circuits Syst. I, 52, 8, pp. 1666-1672, 2005.

[8] H. H. C. Iu and C. K. Tse, Bifurcation Behavior in Parallel-Connected Buck Converters, IEEE Trans. Circuits Systs. I, 48, pp. 233–240, 2001.