2009 International Symposium on Nonlinear Theory and its Applications
NOLTA'09, Sapporo, Japan, October 18-21, 2009

A Clock-Period Comparison ADPLL with a Linearity Improved DCO

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Abstract—We proposed new architecture of phase-locked loop (PLL) by using clock-period comparison. For a digitally controlled PLL, we evaluated the use of a clock-period comparator (CPC). In proposed PLL, only the frequency lock operation should be performed; however, the frequency control by CPC results in the phase lock operation. Thus, the phase lock operation is also simultaneously achieved. We designed element blocks of the proposed PLL using a 0.25-μm CMOS process. We succeeded in digitizing a voltage controlled oscillator (VCO) with a linear characteristic. We also confirmed a phase lock operation by measurement.

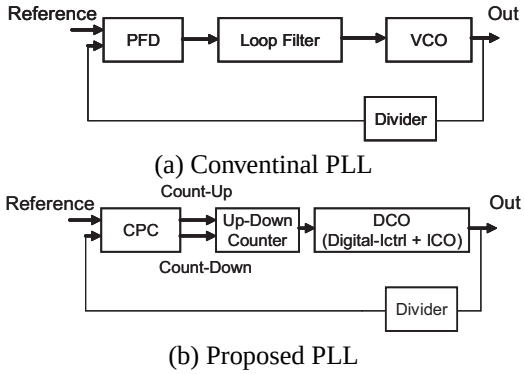

Figure 1: Structure of PLL

1. Introduction

The field of broadband communications has been developing rapidly in recent years as our information-based society continues to expand. Relatively large amounts of data can now be handled with ease, and the exchange of image and music data has become commonplace. In both wired and wireless communications, synchronous technology is indispensable, and this technology is used on various levels, such as the protocol level and circuit level. The phase-locked loop (PLL) was first introduced as a synchronous circuit, and is used for clock recovery, frequency synthesis, and other operations. However, because the PLL was developed with analog elements and a distinctive control mechanism, changing the set circuit parameters has been difficult. In digitizing PLLs, the algorithm for a divider or phase noise reduction was implemented in circuit form over a period of a few decades, after which monolithic implementation with PLL circuits was carried out. In recent years, digital-circuit implementation of the main analog elements in PLLs has progressed, and a voltage controlled oscillator (VCO) and a loop filter have also been implemented in digital circuit form[1]. However, the design of the loop filter that determines the control characteristics of all the PLL's functions requires considerable knowledge and experience, and even if the loop filter is digitized, the design of the loop filter is no less difficult.

In this work, we focused on a phase-frequency detector (PFD) for the digital PLL, and we designed and evaluated the architecture of the PLL, which is not dominated by the loop filter. This PLL compares the clock period of a reference signal and an output signal and performs a phase-lock operation. Since only the phase lock operation is performed by the clock-period comparison, the loop filter can be simplified. Strictly speaking, only the frequency lock operation should be performed; however, the phase lock operation is also simultaneously achieved by performing the clock-period comparison when the phases of the reference signal and the output signal approach each other.

2. Structure of Proposed PLL

2.1. Concept of proposed PLL

The conventional PLL architecture is shown in Fig. 1(a). It consists of a PFD, a charge pump, a loop filter, a VCO, and a divider. A phase difference between a reference signal and an output signal passing through the divider is detected by the PFD. The detected phase difference is input to the charge pump. The charge pump generates current flow, depending on the phase difference. In the loop filter, a control voltage for the VCO is generated by the current flowing from the charge pump. In this way, the PLL performs the phase lock operation.

When the phase is locked, the phase difference is no longer detected. For a conventional phase detector, an XOR circuit and another logical circuit such as a D flip-flop are used with the charge pump. A loop filter is formed by a second or higher-order low-pass filter. Analog elements such

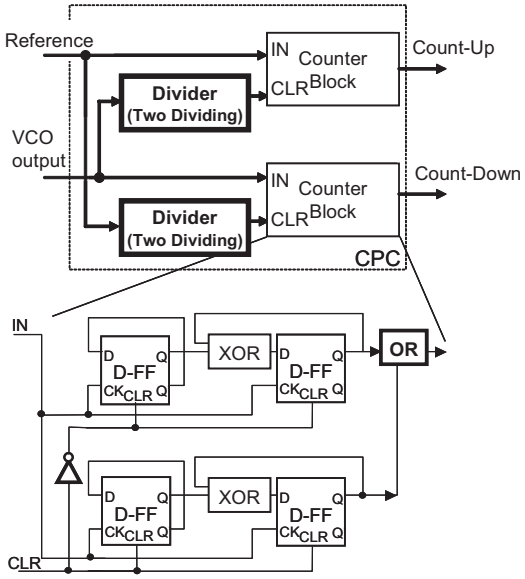

Figure 2: Circuitry of CPC

as capacitors and resistors are used for the loop filter. Analog elements are also used for the VCO.

PLL circuitry consists of many analog elements. Therefore, changes in element parameters during operation and with different applications are problems needing further research. Digital-circuit implementation is a potential solution to these problems.

Our proposed PLL architecture is shown in Fig. 1(b). The PLL performs the phase lock operation by comparing the signal clock periods. This PLL consists of a clock-period comparator (CPC), an up-down counter, a DCO (Digital current controller and ICO), and a divider. A difference in clock period between a reference signal and an output signal passing through the divider is detected by the CPC. The PLL is controlled by the detected clock-period difference. The CPC generates control signals for the up-down counter. The up-down counter generates a control signal for the DCO.

Figure 2 shows the structure of the CPC. The CPC is a frequency detector; therefore, only a frequency lock operation would be expected. However, this PLL also performs phase lock operations. Because the closed-loop operation is performed when phases approach each other (i.e., the clock period on one side that has wrapped around the other side), the phase lock operation is achieved by rapid switching between two quantized points near the point where the phase and frequency differences are zero. The closed-loop operation is not performed continuously. Thus, the effect of the loop characteristic is not dominant.

Table 1 shows a comparison between the proposed PLL and the bang-bang-type PLL with a typical digital phase detector[2, 3, 4]. The loop characteristic of the proposed PLL has a small effect. Therefore, a simple circuit such

Table 1: Comparison between bang-bang-type PLL and proposed PLL

	Bang-Bang	Proposal
Detection scheme	phase	clock period (frequency)
Closed-loop occurrence	continuous	discontinuous
Loop-characteristic influence	dominant	not dominant
Loop filter type	integrator with other elements	only integrator

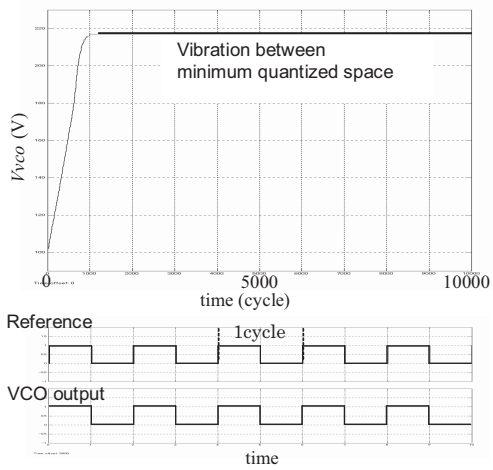

Figure 3: Simulation results of PLL system

as the up-down counter can be used for a loop filter. Moreover, functional expansion can be performed independently of the loop characteristic.

Figure 3 shows the system simulation result of the entire proposed PLL. It was simulated by Simulink by using ideal models of DCO and CPC with counters consisting of D-FF including the delay element. First, the frequency locks based on the response of the control system at the first pole. Afterwards, the up-down event for subordinate position 1-bit space occurs alternately, causing the phase lock.

2.2. Lock-up time of proposed PLL

The pulse occurrence probability of the CPC (the ratio that the closed loop generates) is given as follows. When the clock period of the reference signal is defined to be T_{ref}, and the clock period of the VCO output is defined to be T_{out}, a closed loop for each T_{ref} incidence can be expressed as Eq. (1) in terms of T_{out}. Figure 4 shows a graph of the pulse occurrence probability standardized by $T_{ref} = 1$.

$$P(T_{ref}) = \left|\frac{T_{ref} - T_{out}}{T_{out}}\right| \quad (1)$$

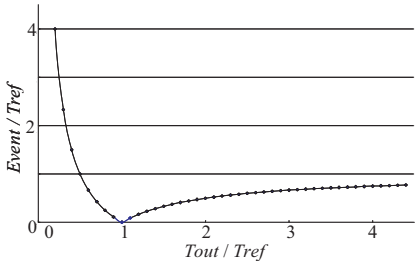

Figure 4: Occurrence probability of closed loop

In the proposed PLL, the pulse occurrence probability has a significant effect on lock-up time. The reciprocal of the above probability is proportional to the time interval in which the pulses are generated. When $T_{ref} < T_{sig}$, the time interval can be given by multiplying the reciprocal of the probability by T_{ref}. When $T_{ref} > T_{sig}$, it can be given by multiplying the reciprocal by T_{sig}.

Moreover, the quantization accuracy is proportional to VCO gain, and it also affects the lock-up time. During the phase-lock operation process, the duration of the pulses expires at quantized intervals. Therefore, lock-up time T_{lock} is expressed as Eq. (2). l denotes the initial counter value; n denotes the counter value at the lock state.

This shows that quantization accuracy and lock-up time are proportional. Therefore, implementing a high-speed lock algorithm by controlling the quantization accuracy is expected.

$$\begin{aligned}(T_{ref} &< T_{out}(k)) \\ T_{lock} &= \sum_{k=l}^{n} |\frac{T_{out}(k)}{T_{ref} - T_{out}(k)}| T_{ref} \\ (T_{ref} &> T_{out}(k)) \\ T_{lock} &= \sum_{k=l}^{n} |\frac{T_{out}(k)}{T_{ref} - T_{out}(k)}| T_{out}(k) \end{aligned} \quad (2)$$

3. Digitally controlled oscillator (DCO)

The standard ring VCO was replaced with a current controller and ring ICO using MOSFETs. In addition, to decrease the circuit delay, the ring VCO with a DAC was replaced with a ring DCO without the DAC by the quantization of the current control segment. Figure 5 shows the circuitry of the ring DCO and a frequency response to a control signal. As for the frequency characteristics of the ring-DCO, secondary nonlinearity appears in the frequency control because the $I - V$ characteristics of the MOSFET have secondary nonlinearity. After attempting to obtain linearity by adjusting the gate width and length of MOSFETs, the resulting frequency response was not completely linear.

Then the linearity of the ring DCO was improved by compensating for the secondary characteristics in the current control segment. The output frequency of the DCO, F, is proportional to n, V, and $n^2 I$. The current flow is quantized by the current mirrors in Fig. 5(c), and the characteristics of current nI_{C1} are given as Eq. (3). Here, $V_c - V_{thP}$ is given as $\sqrt{nI_{C1}/\beta_0}$; therefore, frequency F vs counter value n has square characteristics. Then, we try to cancel the secondary nonlinearity by adding another current mirror as shown in Fig 6. The pMOS current mirrors generate nMOS bias voltage $V_{biasN} - V_{thN}$ as Eq. (4). At that time, if nMOS current mirrors turn on simultaneously, nI_{C1} is given as Eq. (5), $V_c - V_{thP}$ is given as $n\sqrt{I_{C2}/\beta_0}$, and the secondary nonlinearity is compensated. As a result, we succeeded in realizing excellent linear F vs n characteristics in Fig. 7.

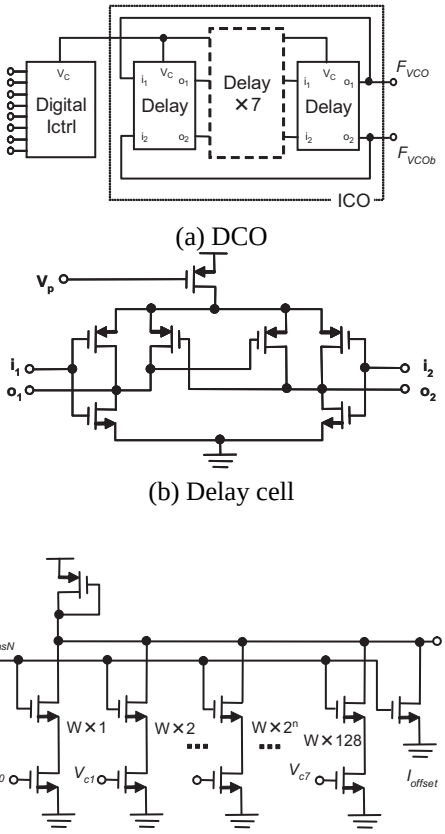

Figure 5: Circuitry of DCO

$$\begin{aligned} nI_{c1} &= \beta_0 (V_c - V_{thP})^2 \\ I_{c1} &= \beta_1 (V_{biasN} - V_{thN})^2 \end{aligned} \quad (3)$$

$$\begin{aligned} I_{c1} = nI_{c2}, I_{c2} &= \beta_2 (V_{biasP} - V_{thP})^2 \\ V_{biasN} - V_{thN} &= \sqrt{n\beta_2/\beta_1}(V_{biasP} - V_{thP}) \end{aligned} \quad (4)$$

$$nI_{c1} = n^2 I_{c2} = \beta_0 (V_c - V_{thP})^2 \quad (5)$$

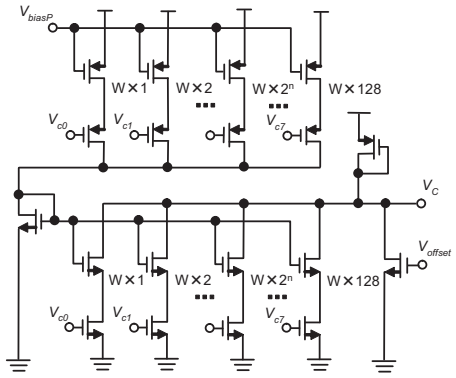

Figure 6: Circuitry of improved digital current controller

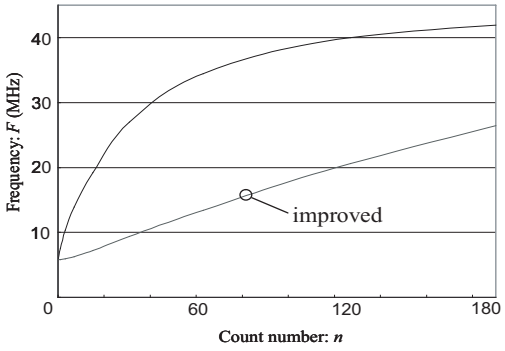

Figure 7: Characteristics of DCO

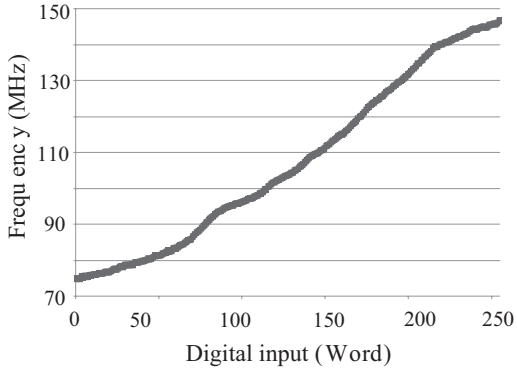

Figure 8: Mesurement result of DCO characteristics

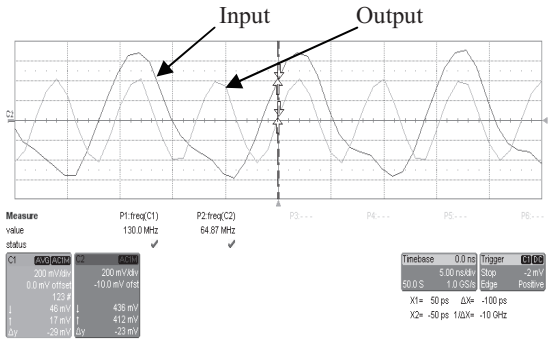

Figure 9: Mesurement result of phase lock operation

4. Measurement

We designed element blocks of the proposed PLL using a 0.25-μm CMOS process. Moreover, we designed a layout pattern for the proposed PLL for a trial circuit.

Figure 8 shows a measurement result of frequency characteristics of the DCO changing digital input. The offset voltage holds on 0.8V. We confirm getting linear characteristics, and DCO range is 75 to 150MHz.

Figure 9 shows the measurement results of the phase lock operation in the trial circuit. The input reference frequency was 65MHz, and the feedback frequency has been divided twice. So the actual output frequency was 130MHz. and we confirmed the phase lock operation.

5. Conclusion

We proposed a digitally controlled PLL with a CPC for the possible realization of frequency and phase locking with a simple integrator. We discussed the principle of the PLL's lock-up time. In addition, we succeeded in digitizing the entire PLL by replacing the VCO with a DCO (Digital current controller and ICO). Moreover, considerable linearity was secured in the ring DCO. Finally, the phase lock operation was confirmed by measurement.

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