2015 International Symposium on Nonlinear Theory and its Applications
NOLTA2015, Kowloon, Hong Kong, China, December 1-4, 2015

Neuromorphic Circuits and Devices exploiting Noise and Fluctuations

Tetsuya Asai and Seiya Kasai

Graduate School of Information Science and Technology, Hokkaido University
Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, Japan

Abstract—This paper provides an overview of the recent development of our noise-driven electrical circuits and devices whose architectures were inspired by biological nervous systems. Noises are inevitable under natural environment, however, one usually tries to "attenuate" noises and fluctuations on semiconductor circuits and devices by using, for example, special shielding equipments, precise fabrication process, special layout or circuit techniques, and so on. On the other hand, biological systems certainly "exploit" noises to increase performances on neural computation. In this paper, some examples of noise-driven neural computing on semiconductor circuits and devices are presented, which may show what noise-driven circuits and systems can do now, and what they may do in the future.

1. Introduction

Noise and fluctuations are usually considered as "obstacles" in the operation of both analog and digital circuits, and most strategies to deal with them are focused on the suppression. This paper gives an overview of neural systems that employ different strategies, i.e., neural strategies that can "exploit" the properties of noise to improve the efficiency of operations. This concept may be especially useful in the design of computing systems with noise-sensitive devices (e.g., extremely low-power but noise-sensitive devices like single electron/molecule devices and subthreshold analog CMOS devices).

Table 1 shows some examples of noise-driven neural processing and their possible applications in electronics. Stochastic resonance (SR) [1] is a phenomenon where a static or dynamic threshold system responds stochastically to a subthreshold or suprathreshold input with the help of noise. In some biological systems SR is utilized to detect weak signals under a noisy environment. SR on some emerging nanoelectronic devices (a SET network and GaAs nanowire FETs) has been demonstrated [5, 6, 7]. SR can be observed in many bi-stable systems, and will be utilized to facilitate the state transitions in emerging logic (bi-stable) memory devices. Noise-driven fast signal transmission is observed in neural networks for the vestibulo ocular reflex [8], where signals are transmitted with an increased rate over a neuronal path when non-identical neurons and dynamic noise are introduced. Implementation in terms of a SET circuit [10] has demonstrated that when several non-identical pulse-density modulators were used as noisy neurons, performances on input-output fidelity of the population increased significantly as compared to that of a single neuron circuit. Phase synchronization among isolated neurons [11] can be utilized for skew-free clock distribution where independent oscillators are implemented on a chip as distributed clock sources, while the oscillators are synchronized by a common temporal noise. Noise in synaptic depression [13] can be used to facilitate the operation of a neuromorphic burst-signal detector, where the output range of the detector is significantly increased by noise. Noise-shaping in inhibitory neural networks [15] has been demonstrated in subthreshold CMOS [16], where static and dynamic noises can positively be taken if one could not remove a certain level of noise or device mismatches. The circuits exploit properties of device mismatches and external (temporal) noise to perform noise-shaping 1-bit AD conversion (pulse-density modulation).

Table 1: Noise-driven neural processing and its possible applications on semiconductor circuits and devices

Neurophysiological phenomena	**Type of noise**	**Applications and device examples**
stochastic resonance [1]	dynamic, static	sensors and logic (CMOS [2, 3], SET [4], GaAs nanowire FET [5, 6, 7])
fast signal transmission on slow transmission pathway [8]	dynamic, static	fast signal transmission, pulse-density modulation (CMOS [9], SET [10])
phase synchronization among isolated neurons [11]	dynamic	phase synchronization among isolated circuits, PLL (CMOS) [12]
synaptic depression [13]	static	burst signal detection (SET) [14]
Noise-shaping in inhibitory neural networks [15]	dynamic, static	noise shaping AD conversion (CMOS [16], SET [17])

In this paper, we introduce two examples among the entries avobe. First, noise-induced synchronization among sub-RF CMOS analog oscillators for skew-free clock distribution [12] is introduced. Independent oscillators are implemented on a chip as distributed clock sources, while the

oscillators are synchronized by a common temporal noise. Second, a high-fidelity pulse-density modulator with noisy neuromorphic circuits based on a model of vestibulo-ocular reflex [9] is introduced. When several non-identical pulse-density modulators are collected as noisy neurons, performances on input-output fidelity of the population is significantly increased as compared with that of a single neuron circuit.

All the components above can be implemented by using standard CMOS processes. These strategies may be important in the designs of emerging computer architectures consisting of nanometer-scale (so noise-sensitive) devices.

2. On-chip CMOS clock generators exhibiting noise-induced synchronous oscillation

Synchronous sequential circuits with global clock-distribution systems are the mainstream of implementation in present digital VLSI systems where the clock distribution is the core of synchronous digital operations. Practical clocks given through external pads are distributed to sequential circuits being synchronous to the same clocks via distributed clock networks. System clocks for synchronous digital circuits must arrive at all the registers simultaneously. In practice, time mismatches of clock arrival which are called 'clock skew' occur in LSIs [18]. The major reasons for these mismatches derive from the system clock distribution (wiring defects or asymmetric clock paths), the propagation delay of the clock chip, and the clock traces on the board. The propagation delay is dependent on the fabrication process, voltage, temperature, and loading, which makes the clock skew even more complicated. Small clock skews prevent us from increasing the clock frequency, and large skews may result in severe malfunctions. Indeed clock-skew effects on the circuit performance rise as the integration density (~miniaturization) or the clock frequency increases.

To resolve these clock-skew issues, various technologies on clock distribution are widely used in present digital systems such as zero-skew clock distribution [19], inserting buffers for skew compensation [20] and controlling the clock-wire length [21]. In regular circuit structures, clock skews are effectively reduced by designing clock paths based on H trees. For large-scale complex clock networks, optimizing buffers in the clock distribution tree usually reduces clock skew. One possible way to cancel clock skew is to use asynchronous digital circuits where only local clocks are used instead of global system clocks . However, the functions of these circuits currently cannot satisfy various sophisticated demands. Moreover, major LSI designers have recently started using advanced genetic algorithms in their post-manufacturing processes to calculate the required margin.

The present solutions for the skew problems may increase both the total length of clock distribution wires and the power consumption, as well as optimization and post-processing costs. Here, we introduce another solution for the skew problems. Nakao *et al.* recently reported that independent neural oscillators can be synchronized by applying appropriate noises to the oscillators [11]. We regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize with the addition of artificial (or natural if possible) noises.

We designed a Wilson-Cowan oscillator circuit for sub-RF operations [12]. The circuit consists of a differential pairand a buffer circuit composed of two standard inverters, and we confirmed the limit-cycle oscillations where the trajectory was effectively fluctuated by the M-sequence circuit with the RC filter. The oscillation frequency was about 1 GHz. All the circuits exhibited independent oscillations when random sequence was not given to them, whereas they exhibited complete synchronization when random sequence was given. Our results indicated that if we distributed these circuits as ubiquitous clock sources on CMOS LSIs, they could be synchronized when common random impulses were given to the circuits. Although this may cancel out the present clock skew problems, device mismatches between the clock sources may prevent the sources from complete synchronization. We also investigated the device-mismatch dependence of the proposed circuits. For our distributing purposes, local mismatches in a single oscillator circuit would be negligible; i.e., mismatches in a differential pair and a current mirror. However, mismatches of bias transistors between the oscillators may drastically change each oscillator's intrinsic frequency.

3. High-fidelity pulse-density modulation with noisy neuromorphic circuits based on a model of vestibulo-ocular reflex

Here we introduce possible ways to construct an electrical circuit that can perform high-speed information processing with slow devices. Regarding this point, neural networks seem to be a possible choice because they are considered to perform high-speed parallel information processing with neuron elements which are relatively slower than CMOS transistors. In recent study, Hospedales *et al.* reported that a neural network with temporal noises and spatial noises in neurons that was used to perform "vestibulo-ocular reflex" (VOR) could conduct a temporal signal whose frequency was higher than operation frequency of a single neuron in networks [8]. VOR stabilizes the visual field by moving the eyeballs in such a way that compensates for rotations of the head. They reported that this function could be achieved by using temporal and spatial noises of neurons. When no noises are applied to this network, all the neurons generate spike output at the same time (phase). However, when they are affected by temporal noises and spatial noises, they no longer can generate spike output at the same time. It represents that the net-

work shows asynchronous firing and it can thus respond to relatively faster input signal than a single neuron.

The operation frequency in electrical circuits of a single device is limited by several conditions that derive from physical limitations. Electrical circuits are often limited by power consumption or chip area size especially in mobile appliances or sensor appliances. Information processing done by the brain is considered to have an energy-efficient structure. The architecture observed in the brain may provide possible solutions to electrical engineering. Further more, electrical-circuit engineers often try to reduce or eliminate the effects of noises and device mismatches of transistors because these effects degrade circuit characteristics and they even cause erroneous circuit operation. Typical circuit designs to reduce these effects often require additional transistors and larger transistors (larger chips and greater power consumption), which makes it more difficult to meet the specification. Here, by implementing Hospedales et al.'s model in electrical circuits, noises and device mismatches in these circuits could be utilized to improve operations while group of slow devices could achieve faster operation. We constructed a simple neural-network circuit to confirm the improvements in fidelity and we then demonstrate that the operation frequency of a noisy network circuit is higher than that of a noiseless network circuit [9].

4. Summary

In this paper, a brief review of noise-driven neural processing and their applications were introduced.

First, an overview of noise tolerance and noise utilization in neural systems and their possible application in electronics was introduced. Noise and fluctuations are usually considered obstacles in the operation of both analog and digital circuits and systems, and most strategies to deal with them focus on suppression. Neural systems, on the other hand, tend to employ strategies in which the properties of noise are exploited to improve the efficiency of operations. This concept may be especially useful in the design of computing systems with noise-sensitive devices.

Second, we introduced CMOS sub-RF oscillators that could be synchronized using common random impulses, based on a theory in [11]. The synchronization properties of the modified model were qualitatively equivalent to those of the original model. A sub-RF oscillator circuits based on the modified model was designed. The circuits exhibited the same synchronization properties as in the original and modified models. For our clock-distributing purposes, synchrony dependence on device mismatches between the distributed oscillator circuits was investigated. The result showed that the synchrony was gradually decreased when variance of the mismatch was linearly increased, which indicated that our 'ubiquitous' clock sources with small device mismatches would be synchronized by optimizing our parameter sets.

Finally, we introduced a neuromorphic circuit with high fidelity in its output spike train based on the Vestibulo-Ocular Reflex model. The network circuit was composed of neuron circuits, an M-sequence circuit, and an OR logic circuit. A single neuron circuit could operate up to $O(10^2)$ Hz and it operated incorrectly over the frequency. When four neurons were employed, the network without noises had the same characteristics while the network with noises had higher performance than that without noises. The noisy network could operate correctly at $O(10^3)$ Hz and we confirmed that fidelity could be increased by noises. We were forced to limit the operation frequency of the neuron circuit that we introduced here forced to a certain value due to the size of capacitance in the circuit. We plan to use a subthreshold CMOS circuit that allows an ultra-low power circuit even though device mismatches strongly degrades circuit characteristics.

We have extended our noise-driven CMOS circuits to "single-electron circuits" towards their application to "single-molecule devices", that are much more sensitive to both external and internal (thermal) noises, e.g., single-electron neural network for synchrony detection [14], stochastic resonance in single-electron circuits [22, 5], single-electron circuits performing dendritic pattern formation with nature-inspired cellular automata [23], single-electron image processing architectures for edge detection [24] and motion detection [25], a noise-shaping single-electron pulse-density modulator [17], and so on.

Acknowledgments

This study was supported by a Grant-in-Aid for Scientific Research on Innovative Areas [2511001503] from the Ministry of Education, Culture, Sports, Science and Technology (MEXT) of Japan.

References

[1] L. Gammaitoni, P. Hanggi, P. Jung, and F. Marchesoni, "Stochastic resonance," *Reviews of Modern Physics*, vol. 70, no. 1, pp. 223-287, Jan. 1998.

[2] A. Utagawa, T. Asai, and Y. Amemiya, "Stochastic resonance in simple analog circuits with a single operational amplifier having a double-well potential," *Nonlinear Theory and Its Applications*, vol. 2, no. 4, pp. 409-416, Oct. 2011.

[3] L. Gonzalez-Carabarin, T. Asai, and M. Motomura , "Application of nonlinear systems for designing low-power logic gates based on stochastic resonance," *Nonlinear Theory and Its Applications*, vol. 5, no. 4, pp. 445-455, Jan. 2014.

[4] T. Oya, A. Schmid, T. Asai, and A. Utagawa, "Stochastic resonance in a ballanced pair of single-

electron boxes," *Fluctuation and Noise Lett.*, vol. 10, no. 3, pp. 267-275, Sep. 2011.

[5] S. Kasai and T. Asai, "Stochastic resonance in Schottky wrap gate-controlled GaAs nanowire field effect transistors and their networks," *Applied Physics Express*, vol. 1, no. 8, p. 083001, Aug. 2008.

[6] S. Kasai, K. Miura, Y. Shiratori, "Threshold-variation-enhanced adaptability of response in a nanowire field-effect transistor network," *Appl. Phys. Lett.*, vol. 96, no. 194102, 2010.

[7] Y. Imai, M. Sato, T. Tanaka, S. Kasai, Y. Hagiwara, H. Ishizaki, S. Kuwabara, and T. Arakawa, "Detection of weak biological signal utilizing stochastic resonance in a GaAs-based nanowire FET and its parallel summing network," *Jpn. J. Appl. Phys.*, vol. 53, p. 06JE01, 2014.

[8] T. M. Hospedales, M. C. W. van Rossum, B. P. Graham, and M. B. Dutia, "Implications of noise and neural heterogeneity for vestibulo-ocular reflex fidelity", *Neural Computing*, 20, 3, 756–778, 2008.

[9] A. Utagawa, T. Asai, and Y. Amemiya, "High-fidelity pulse density modulation in neuromorphic electric circuits utilizing natural heterogeneity," *Nonlinear Theory and Its Applications*, vol. 2, no. 2, pp. 218-225, Apr. 2011.

[10] A.K. Kikombo, T. Asai, and Y. Amemiya, "Neuromorphic circuit architectures employing temporal noises and device fluctuations to improve signal-to-noise ratio in a single-electron pulse-density modulator," *Int. J. Unconventional Computing*, vol. 7, nos. 1-2, pp. 53-64, Sep. 2011.

[11] H. Nakao, K. Arai, and K. Nagai, "Synchrony of limit-cycle oscillators induced by random external impulses," *Phys. Rev. E*, vol. 72, 026220, 2005.

[12] A. Utagawa, T. Asai, T. Hirose, and Y. Amemiya, "Noise-induced synchronization among sub-RF CMOS analog oscillators for skew-free clock distribution," *IEICE Trans. Fundamentals*, vol. E91-A, no. 9, pp. 2475-2481, Sep. 2008.

[13] W. Senn, I. Segev, and M. Tsodyks, "Reading neuronal synchrony with depressing synapses," *Neural Computation*, vol. 10, no. 4, pp. 815-819, Apr. 1998.

[14] Oya T., Asai T., Kagaya R., Hirose T., and Amemiya Y., "Neuronal synchrony detection on signle-electron neural network," *Chaos, Solitons and Fractals*, vol. 27, no. 4, pp. 887–894 (2006).

[15] D.J. Mar, C.C. Chow, W. Gerstner, R.W. Adams, and J. . Collins, "Noise shaping in populations of coupled model neurons," *Neurobiology*, 96, pp. 10450-10455, 1999.

[16] A. Utagawa, T. Asai, T. Hirose, and Y. Amemiya Y., "An inhibitory neural-network circuit exhibiting noise shaping with subthreshold MOS neuron circuits," *IEICE Trans. Fundamentals*, vol. E90-A, no. 10, pp. 2108-2115, Oct. 2007.

[17] Kikombo A.K, Asai T., Oya T., Schmid A., Leblebici Y., and Amemiya Y., "A neuromorphic single-electron circuit for noise-shaping pulse-density modulation," *International Journal of Nanotechnology and Molecular Computation*, vol. 1, no. 2, pp. 80–92 (2009).

[18] D.E. Brueske and S.H.K. Embabi, "A dynamic clock synchronization technique for large systems," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 17, pp. 350-361, 1994.

[19] R.S. Tsay, "An exact zero-skew clock routing algorithm," *IEEE Trans. on Comp.-Aided Design of Integrated Cir. Syst.*, vol. 12, no. 2, pp. 242-249, 1993.

[20] R.B. Watson, Jr., and R.B. Iknaian, "Clock buffer chip with multiple target automatic skew compensation," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1267-1276, 1995.

[21] T.-H. Chao, Y.-C. Hsu, J.-M. Ho, and A.B. Kahng, "Zero skew clock routing with minimum wirelength," *IEEE Trans. Circuits and Systems II*, vol. 39, no. 11, pp. 799-814, 1992.

[22] Oya T., Asai T., and Amemiya Y., "Stochastic resonance in an ensemble of single-electron neuromorphic devices and its application to competitive neural networks," *Chaos, Solitons and Fractals*, vol. 32, no. 2, pp. 855–861 (2007).

[23] Oya T., Motoike I.N., and Asai T., "Single-electron circuits performing dendritic pattern formation with nature-inspired cellular automata," *International Journal of Bifurcation and Chaos*, vol. 17, no. 10, pp. 3651–3655 (2007).

[24] Kikombo A.K., Schmid A., Asai T., Leblebici Y., and Amemiya Y., "A bio-inspired image processor for edge detection with single-erectron circuits," *Journal of Signal Processing*, vol. 13, no. 2, (2009), in press.

[25] Kikombo A.K., Asai T., and Amemiya Y., "An elementary neuro-morphic circuit for visual motion detection with single-electron devices based on correlation neural networks," *Journal of Computational and Theoretical Nanoscience*, vol. 6, no. 1, pp. 89–95 (2009).