3-Input 2-Output Comparator Based on Rail-to-Rail Operational Amplifier using Subthreshold Region

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Abstract– In this paper, I propose, design and evaluate 3-input 2-output comparator circuit based on rail-to-rail operational amplifier using subthreshold region. Proposed circuit has additional pMOSFET and nMOSFET input pair and cascade output circuit. As the results, less than a few MHz operations at 0.5V power supply can be achieved.

1. Introduction

For low speed (less than a few MHz) sensor systems, such as gas detector, and pressure sensor, it is very important to reduce power consumption because of a long-term operation. One of the method of reducing power is to design using subthreshold region [1-3].

To achieve power consumption for analog signal processing, I proposed PWM analog differential inputs operational circuit [4]. Fig.1 shows PWM analog differential operational circuit. Vin1 and Vin2 are the analog signal input. Two analog signals are translated and generated to PWM signals using triangle or sawtooth wave in comparator circuits. Converted signals are calculated to the absolute value by EXOR. EXOR output is represented as the pulse width proportional to the absolute value of the Vin1-Vin2 like analog differential operation. EXOR signal is entered to current amplifier using large width MOSFETs. Final output will be square wave with the time axis information, but connected off-chip integral circuit, which is designed by capacitor and resistor, can be restored analog signal. Proposed circuit has mixed signal architecture and can be achieved the same performance as ultra-low voltage analog amplifier, under 1uW@1MHz under 0.5V power supply.

However, PWM generator uses two rail-to-rail operational amplifiers. Fig.2 shows the 3-input 2-output rail-to-rail comparator using two operational amplifiers. The circuit size is very large and variation characteristic of each comparator may have problem.

In this paper, I propose and evaluate 3 input 2 output analog comparator based on only one simple rail-to-rail operational amplifier.

2. The circuit architecture and principles

2.1 The circuit architecture

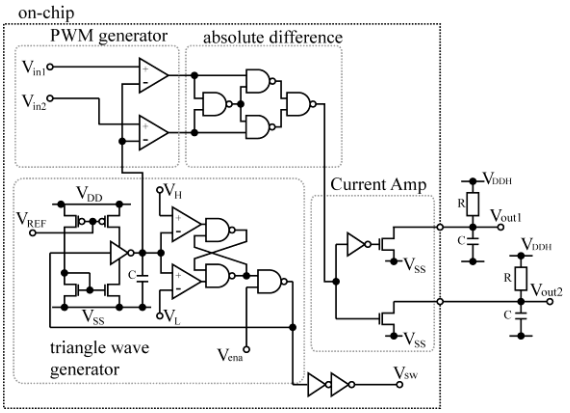

Fig.1 0.5V PWM differential operational circuit

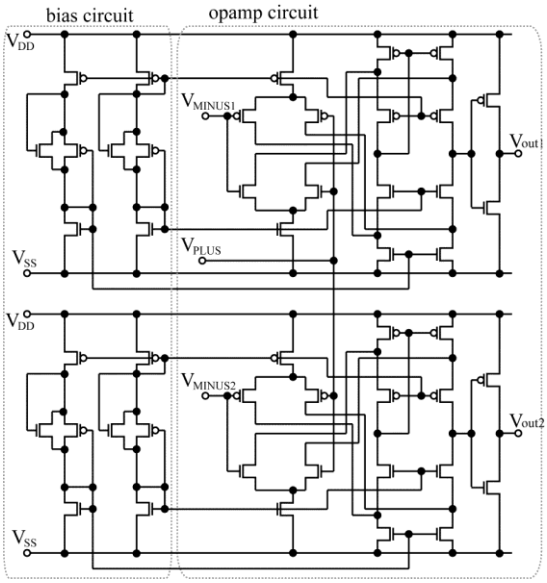

Fig.2 3-Input 2-Output comparator using two comparators

Fig.3 shows the circuit architecture of proposed 3-input 2-output rail-to-rail comparator. This circuit has additional one pMOSFET and nMOSFET input pair and one cascade output circuit. V_{PLUS} has common analog input signal, and V_{MINUS1} and V_{MINUS2} have another analog signal. V_{out1} produces the result of comparison between V_{PLUS} and V_{MINUS1}, and V_{out2} produces the result of comparison between V_{PLUS} and V_{MINUS2}. V_{out1} and V_{out2} are generated at the same time.

A number of MOSFETs in fig.3 and fig.2 are 22 and 48, respectively. Proposed circuit can be reduced about the half larger than two parallel analog amplifiers.

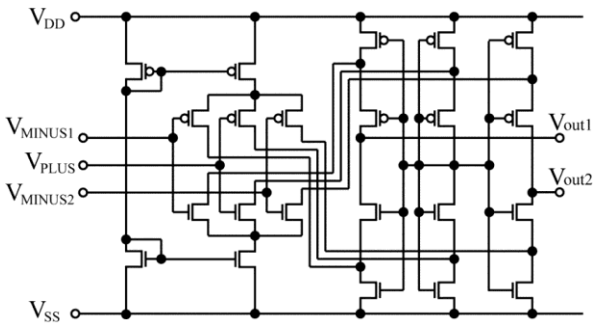

Fig.3 Proposed 3-input 2-output comparator

2.2 The principles

This circuit operates under the subthreshold region. The equation of subthreshold operation is as follows [5].

$$I_D = I_o exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \quad \dots (1)$$

,

which I_O is a process parameter, such as L, W, μ, and etc., and V_{GS}, V_{th}, n, and V_T are gate voltage, threshold voltage, n factor, and thermal voltage, respectively. From the equation (1), subthreshold current is exponential of gate voltage.

Fig.4 shows an equivalent circuit of 3-input 2-output comparator. V_1 has common analog input signal, and V_2 and V_3 have another analog signal. ΔI_2 produces the result of comparison between V_1 and V_2, and ΔI_3 produces the result of comparison between V_1 and V_3. From the equation (1) for each MOSFETs, ΔI_2 and ΔI_3 are expressed as follows:

$$\Delta I_2 = I_2 - I_1 = I_b \frac{exp\left(\frac{\Delta V_2}{nV_T}\right) - 1}{1 + exp\left(\frac{\Delta V_2}{nV_T}\right) + exp\left(\frac{\Delta V_3}{nV_T}\right)} \quad \dots (2)$$

and

$$\Delta I_3 = I_3 - I_1 = I_b \frac{exp\left(\frac{\Delta V_3}{nV_T}\right) - 1}{1 + exp\left(\frac{\Delta V_2}{nV_T}\right) + exp\left(\frac{\Delta V_3}{nV_T}\right)} \quad \dots (3)$$

,

which

$$\left.\begin{array}{l} \Delta V_2 = V_2 - V_1 \\ \Delta V_3 = V_3 - V_1 \\ I_b = I_1 + I_2 + I_3. \end{array}\right\} \quad \dots (4)$$

From the equation (2) and (3), if $V_2 = V_1$ or $V_3 = V_1$, ΔI_2 and ΔI_3 are zero, respectively. But, if $V_2 > V_1$ or $V_2 < V_1$, ΔI_2 is equal to negative or positive value like hyperbolic tangent of ΔV_2 (=V_2 - V_1). If $V_3 > V_1$ or $V_3 < V_1$, ΔI_3 is also equal to negative or positive value like hyperbolic tangent of ΔV_3 (=V_3 - V_1).

Thus, by defining large or small state as negative value or positive value, 3-input 2-output comparator can output the results of two comparison data between V_1 and V_2 and between V_1 and V_3 at the same time.

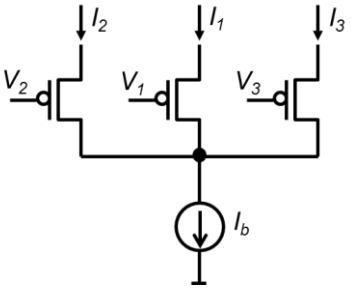

Fig.4 Equivalent circuit of 3-input 2-output comparator

3. Simulation results

This circuit is designed and evaluated by using 65 nm CMOS process technology. Power supply voltage (V_{DD}) is set to 0.5V. In this simulation, corner evaluation are applied, such as SF (slow nMOS and fast pMOS), FS (fast nMOS and slow pMOS), and TT (typical nMOS and pMOS). In this evaluation, unity-gain frequency and input-output transfer characteristics are used because they are important for determining the maximum operation frequency and comparison characteristics.

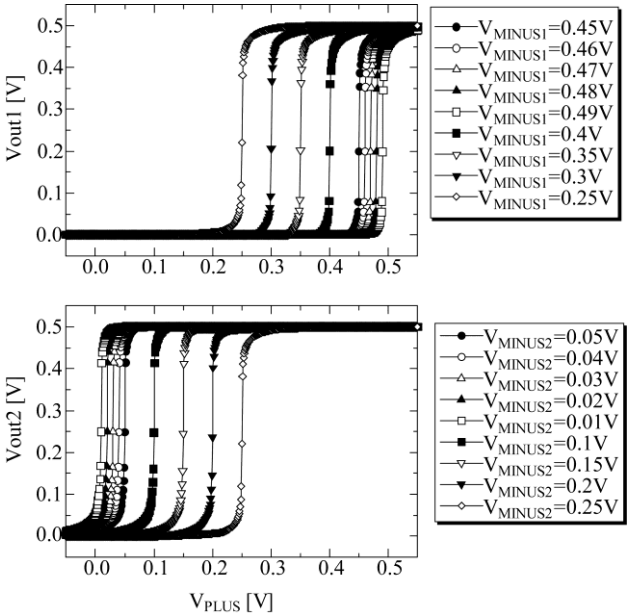

Fig.5 Input-output transfer characteristics

Fig.5 shows the results of the output characteristics of Vout1 and Vout2. Fig.6 shows the results of frequency characteristics when V_{MINUS1}=0.45V and V_{MINUS2}=0.05V, and fig.7 shows the results of frequency characteristics when V_{MINUS1}=V_{MINUS2}=0.25V, respectively.

From fig.5, V_{out1} and V_{out2} are the results of comparison operation between V_{PLUS} and V_{MINUS1} and between V_{PLUS}

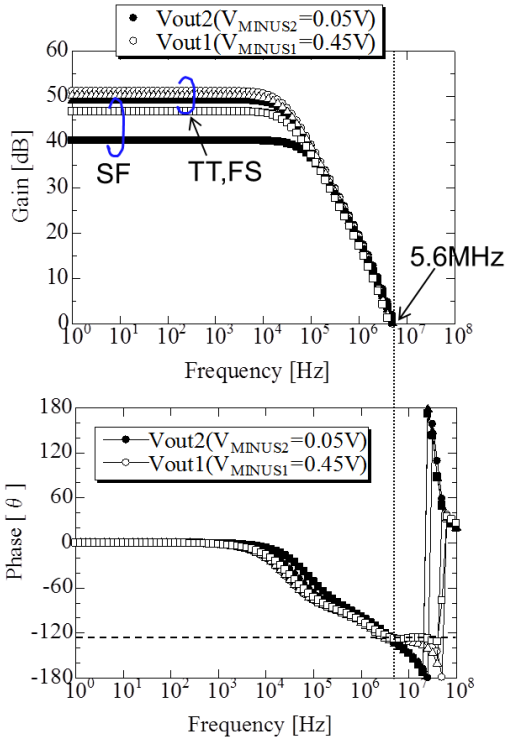

Fig.6 Gain and phase characteristics @ V_{MINUS1} is not equal to V_{MINUS2}

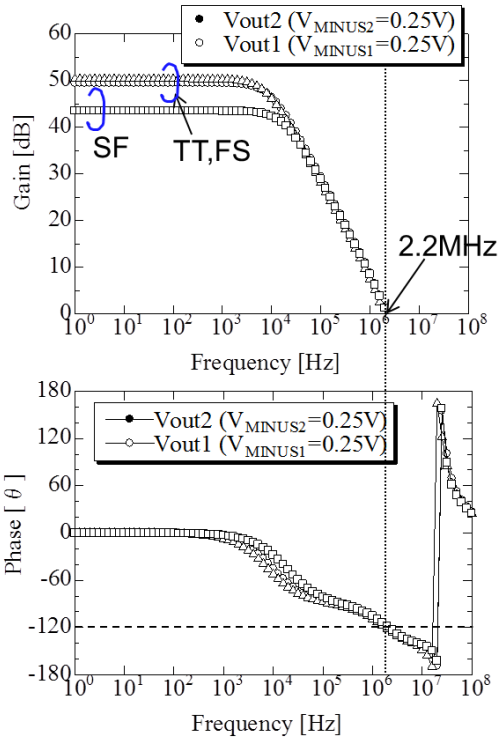

Fig.7 Gain and phase characteristics @ V_{MINUS1}=V_{MINUS2}

and V_{MINUS2}, respectively. V_{out1} and V_{out2} can realize simultaneous and non-inverted outputs. In addition, the gain of this circuit is almost high from the gradient of input-output transfer characteristic.

From fig. 6 and 7, in case of differential V_{MINUS1} and V_{MINUS2}, unity-gain frequency is the same as 5.6 MHz. Nevertheless, in case of V_{MINUS1}=V_{MINUS2}, unity-gain frequency is decreasing to 2.2 MHz. Because three pair of input MOSFETs flow the same bias currents, operation current is lower. As a result, unity-gain is also lower. When a difference between V_{MINUS1} and V_{MINUS2} is increased, unity-gain frequency is increased. The maximum power consumption is 71.0nW from input-output transfer operation.

4. Conclusion

In this study, I designed and evaluated 3-input 2-output comparator circuit. This circuit has additional one pMOSFET and nMOSFET input pair and one cascade output circuit. In fig.3, V_{PLUS} has common analog input signal, and V_{MINUS1} and V_{MINUS2} have another analog signal. V_{out1} produces the result of comparison between V_{PLUS} and V_{MINUS1}, and V_{out2} produces between V_{PLUS} and V_{MINUS2}. As results, two outputs, V_{out1} and V_{out2}, can be generated the results of comparison at the same time. The maximum power consumption is 71.0nW.

Acknowledgments

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