

Cellular Hardware Platform:CAM² on FPGA

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Abstract—In this work, cellular automata on content addressable memory (CAM²) is implemented on FPGA, which is highly parallel two-dimensional cellular automata architecture. It can achieve various cellular automata (CA) processing such as pixel level snakes, morphological wavelet transform and pattern spectrum. These applications are currently offered on ASIC. CAM² on ASIC cannot change its capacity and configuration, while in contrast, CAM² on FPGA is flexible in terms of capacity and configuration, can perform optimum processing, and is low cost. As a result, max frequency and capacity of CAM² on FPGA is respectively fourth and one eighth that of, CAM² on ASIC. Capacity frequency product realizes one twice as much as CAM² on ASIC. CAM² on FPGA is thus poised to make a significant contribution to the development of compact, high-performance systems.

1. Introduction

CAM² is a highly parallel two-dimensional cellular automata architecture [1], [2], [3] that can realize various CA-based processing such as pixel level snakes [4], morphological wavelet transform [5], [6], and pattern spectrum [7], [8]. However, CAM² on ASIC has serious issues; namely, its capacity and configuration cannot be changed, and the cost of developing a new CAM² has become huge. In contrast, FPGA has continued to advance. If CAM² is implemented on FPGA, it becomes an accelerator of various CA-based processes. Moreover, CAM² on FPGA can change its capacity and configuration, and it keeps expenses below that of ASIC. Therefore, CAM² on FPGA is a very appealing platform.

This paper is organized as follows. First, we introduce cellular hardware platforms: CAM² and give an example of its application on ASIC. In sect. 3, CAM² on FPGA is described and the differences between CAM² on FPGA and CAM² on ASIC are discussed. In sect. 4, implementation results of CAM² on FPGA is shown. We conclude with a brief summary in sect. 5.

2. Cellular Hardware Platform

2.1. CAM²

CAM² is being developed for several digital appliances and is composed of content addressable memory (CAM), that makes it possible to embed within it a large number

of processing element (PEs) corresponding to Cellular Automata (CA) cells. Table .1 list the specifications of the CAM² processor and Fig. 3 is photograph of CAM² on FPGA. The CAM² is a compact, high-performance, flexible, and highly parallel 2-D cellular automata. In light of the above, real-time morphological pattern spectrum processing can be realized with the CAM² evaluation system. The CAM² evaluation system and a block diagram of CAM² are shown in Fig. 1 and the CAM cell of CAM² on ASIC is shown in Fig. 2. The CAM² evaluation system consists of a CAM² processor, a FPGA that controls the evaluation board, various memories, a monitor, and a host PC. The most prominent features of the configuration are the dedicated CAM blocks, included in the CAM² processor for the highly parallel PE array. Each CAM block performs various types of parallel data processing for CA in each word. Moreover, the CAM² processor can be easily controlled by command sequences generated from the FPGA. Since the FPGA can easily rewrite the logic, CAM² can perform various types of CA-based image processing either alone or in combination with another system.

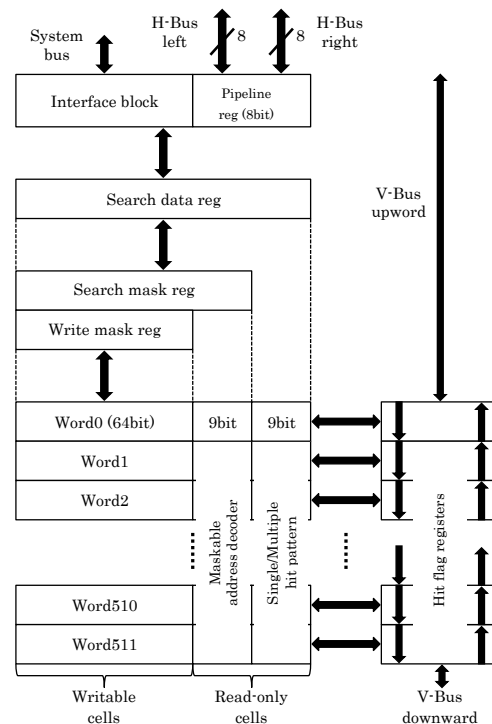


Figure 1: CAM² on ASIC configuration

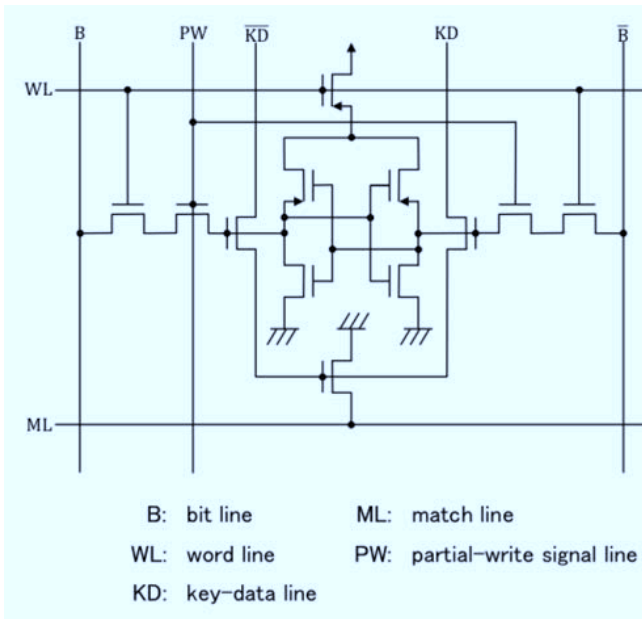


Figure 2: CAM² cell on ASIC

Table 1: specification of CAM² processor

Configuration	512 words × 64 bits × 32 blocks
Instruction set	32
Operating frequency	40 MHz
LSI process technology	0.25 μm CMOS double Al layers



Figure 3: CAM² on ASIC

While the CAM² processor is suitable for CA processing, it also enables effective parallel bit-serial cipher processing that consists of logic operations and table-lookup

coding. CA and cipher processing with the CAM² processor are carried out by iterative data transfer and update operations. To perform the above processing, the following functions are absolutely essential: maskable OR search (A), maskable parallel write (B), and hit-flag shift up down (C). In the case of CA processing, the value of the original cell is transferred to its nearest neighboring cell. In the CA-value update process, the next value of the original cell is calculated by a transition rule using the original and nearest neighboring cell values.

- (A) Maskable OR search
Search data from input are compared with word contents. The maskable search results are accumulated in hit-flag registers through OR logic.
- (B) Maskable partial-parallel write
Data are written into specific bit positions of multiple word locations.
- (C) Hit-flag shift up and down
The hit-flag registers are shifted to upper or lower words.

Through the iteration of these functions, the CA-value transfer and update processes can be carried out in a bit-serial, word-parallel manner. The processing drawbacks are that it takes a long time for such complex operations as the multiplication of longer bits. Moreover, the processing time for the CA-value transfer is proportional to the transfer bit length. Thus, a low-bit CA-value update is required to shorten the processing time.

2.2. Application of CAM²

(A) **Cellular neural network [9],[10]**
In a cellular neural/nonlinear network (CNN), information processing is done in parallel through network dynamics, which means CNN has the potential to realize a highly parallel real-time information processing system. To demonstrate the flexibility and programmability of CAM², nonlinear template CNN was implemented.

(B) **Pixel level snakes [4]**
The snakes algorithm was originally formulated as a variational method. Using the Euler-Lagrange method, it can be transformed into a partial differential equation that can be related to cellular network models. In PLS, the authors developed this model to connect with CNN more easily, and succeeded in leading the snakes algorithm to pixel level cellular computation. In PLS, an external potential is calculated with the gradient of the original image. An active contour dynamically deforms its shape with both its internal energy and the external potential. In the initial state, an active closed curve is given to enclose objects. The shape of the active closed curve iterates the

deformation and the active closed curve contracts until both the internal energy and the external potential are equivalent. When the internal energy and the external potential are reasonable, the equilibrium point of the active closed curve is the contour image of the object.

(C) Morphological wavelet transform [5], [6]

Morphological wavelet transform is wavelet transform based on max-plus algebra. Morphological wavelet transform is not affected by any restrictions regardless of the type of sampling windows. Morphological processing on the CAM² using various structure elements has already been proposed.

(D) Morphological pattern spectrum-based image manipulation detector [7], [8]

The CAM² can realize real-time parallel image-manipulation detection and 1,024-parallelism AES processing. For verifying the effectiveness of the proposed image-manipulation method with the CAM², two types of benchmark images are analyzed by the proposed detection method. The number of clock cycles of the CAM² is up to 58% lower than that of conventional processors. Consequently, the proposed image-manipulation detector with the CAM² implementation is very effective for the investigation of crimes and photographic evidence.

3. CAM² on FPGA

The main benefits of CAM² on FPGA are its flexibility and low cost. In the case of CAM² on ASIC, bit length, number of words, and number of blocks are respectively fixed at 64 bits, 512 words, and 32 blocks. In contrast, CAM² on FPGA can change its configuration and capacity. For example, word can be changed from 64 bits to 32 bits and the number of blocks can be changed to from 16 to 32.

This flexibility can result in better processing. FPGA can also change the configuration and capacity if we change the IP. The CAM² cell on FPGA is shown in Fig. 4. The big difference between CAM² on ASIC and CAM² on FPGA is the CAM cell: on ASIC, it has little flexibility, and on FPGA, it has excellent flexibility, as shown in Fig. 4. The function of CAM² on FPGA was implemented as follows. The maskable OR search takes exclusive OR of the key data and cell data and takes logical conjunction of its result and the search mask. Next, the maskable partial-parallel write takes the logical conjunction of the word line and partial-write signal line. Hit-flag shift up and down is constant to ASIC. These functions are realized easily.

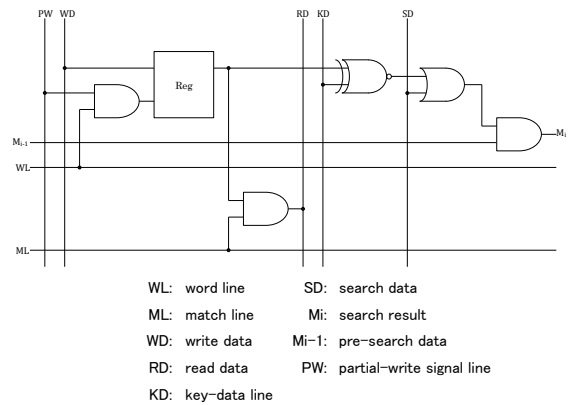


Figure 4: CAM² cell on FPGA

4. Implementation results

CAM² on FPGA is estimated to use three types of FPGA: Spartan-6, Kintex-7, and Virtex-7. A picture of Virtex-7 is shown in Fig. 5. The CAM² on ASIC is 40 MHz and has a 32-block configuration. The maximum capacities of each FPGA are 128 words × 8 blocks (Spartan-6), 512 word × 4 blocks (Kintex-7), and 512 words × 4 blocks (Virtex-7). The maximum implemented capacity of FPGA is smaller by one eighth than ASIC.

The max frequency of FPGA is smaller by 10% when the configuration becomes double blocks and smaller by 20% when it becomes double words. The maximum frequency of FPGA is fourth bigger than ASIC. From these results, multiply max frequency and capacity are about one twice.

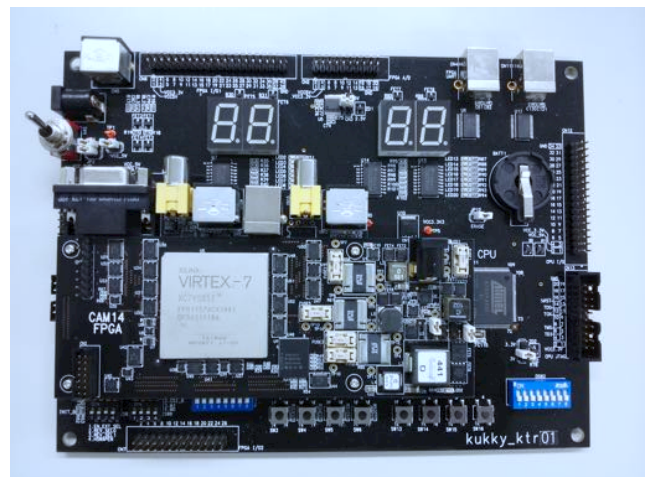


Figure 5: CAM² on FPGA

Table 2: Implementation results

Spartan-6(XC6SLX150)		
word × block	used resource	Max frequency(MHz)
128 × 2	44%	89
128 × 4	84%	82
128 × 8	87%	71

Kintex-7(XC7K480T)		
word × block	used resource	Max frequency(MHz)
256 × 8	90%	205
512 × 4	93%	177

Virtex-7(XC7V585T)		
word × block	used resource	Max frequency(MHz)
256 × 8	73%	205
512 × 4	75%	177

5. Conclusion

In this paper, we discussed our implementation of CAM² on FPGA. CAM² has previously been used to conduct processes such as pixel level snake, morphological wavelet transform, and pattern spectrum. CAM² is implemented on FPGA, on which it can change its capacity and configuration and realize a low cost. The biggest difference between CAM² on ASIC and on FPGA is the CAM cell. Simulations showed that the CAM² on FPGA achieves approximately four times the frequency compared with on ASIC, and the capacity became one eighth. Hence, using state of the art FPGA, CAM² on FPGA becomes larger and larger. CAM² implemented on FPGA has great potential as the accelerator of various CA-based processes.

Acknowledgments

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