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A simple aVLSI burst silicon neuron circuit

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Abstract—Silicon neuron, electrical circuit that reproduces neuronal phenomena, has being designed by copying some biological neuron models themselves. Because of incompatibility between protein-based and silicon-based systems, its circuitry tends to be very complex when we implement conductance-based neuron model. Of course circuitry can be quite simple when we implement simple model such as leaky integrate-and-fire model, but the system dynamics is limited. In our previous works, we proposed another design method to solve this problem, which is to copy mathematical structures in theoretical models. We introduce an aVLSI silicon neuron circuit with relatively simple circuitry that has ability to generate burst firing pattern.

1. Introduction

Brain and nerve systems in creatures are processing huge amount of incoming information and generating appropriate responses in real time. Their computing ability is thought to defeat conventional artificial computing system. It is expected that advanced computing system can be realized by mimicking anatomical and functional structures in brain and nerve systems. An approach to do this is construction of silicon neural network. It is composed of silicon neuron and synapse circuits that correspond to neuronal cell and synapse, respectively.

Electrical circuit that functions similarly to neuronal cell has been realized by implementing solver circuit for some neuron models. If we select a complex conductance-based neuron model such as the leech heart interneuron model[1], the circuitry becomes quite complex and power consumption tends to be high. This is because they try to solve the differential equations of protein-based systems, which is incompatible with silicon-based ones. If we select a simple phenomenological model such as leaky integrate-and-fire neuron model[2], we obtain very simple and low-power-consumption circuit, but the ability to generate dynamical behavior is limited.

To solve this trade-off, we proposed a new design method, "mathematical-model-based design method", in our previous works [3]-[5] where designers copy mathematical structures in neuron models instead of their precise equations. Because designers can utilize silicon-native curves to construct the system equations, the circuitry becomes simple. Theoretical studies on neuron models have been elucidated the essential mechanisms lying under various phenomena in neuronal cells. One of their most successful results is that they explained the mechanism lying under Hodgkin's classification[7] utilizing nonlinear dynamics and bifurcation theory. The generation mechanisms of some types of burst firings are also explained by them[6].

In this work, we introduce a simple silicon neuron circuit with capability of burst firing that is designed for and implemented with complementary metal oxide semiconductor field effect transistor (CMOS FET) analog very-large-scale integrated (VLSI) circuit technology. In this circuit, every FET is operated in subthreshold region to reduce power consumption down to about some μ watts. It has ability to realize several types of burst firing including square-wave burst.

2. Mathematical structure of square-wave burster

Theoretical studies indicated that bifurcation analysis of neuron model reveals its dynamical properties effectively. When the bifurcation parameter is the strength of stimulus current, we can overview what kind of dynamical behaviors are possible in the model. It is well known that type of bifurcations observed in the analysis tells us the model's neuron class (Hodgkin's classification). For example, if a limit cycle emerges via Hopf bifurcation, it starts with a certain non-zero frequency. Then the model is classified as Class II. If a limit cycle emerges via saddle-node on invariant circle bifurcation, it has arbitrarily low frequency. Then the model is classified as Class I. In this case, we can tune some parameters such as time constants of recovery variable (e.g. slow ionic variable) so that the limit cycle emerges earlier (where the stimulus current is weaker). This kind of modification allows the branches of stable and unstable manifolds for the saddle point to merge before the saddle vanishes via saddle-node on invariant circle bifurcation. This produces a homoclinic orbit that connects the saddle point to itself, which turns to a stable limit cycle whose frequency is arbitrarily low. Because the stable node that represents the resting state survives this bifurcation, there arises bistability between these two stable states, a limit cycle and a node. If we apply negative feedback current that depends on the membrane potential to systems with such bistability, burst firing is observed. This type of burst firing is called square-wave burst because the waveform of membrane potential is in square shape. The neg-

ative feedback current has some biological counterpoints. Calcium dependent potassium current (I_{K-Ca}) is a good example, which passes through potassium channel that opens when calcium concentration in the cell becomes high.

3. Silicon neuron circuit

We reproduced the mathematical structure described in the previous section utilizing silicon-native curves. For low power consumption, we operated MOSFETs in subthreshold region, where the most silicon-native curve is hypertangent. Our system equations are as follows:

$$C_y \frac{dy}{dt} = -g_y(y) + f_m(y) - n + I_a + I_f + I_{stim}, \quad (1)$$

$$C_n \frac{dn}{dt} = f_n(y) - n, \quad (2)$$

$$C_q \frac{dq}{dt} = f_p(y) - q, \quad (3)$$

$$I_f = I_c - q, \quad (4)$$

where y and n represent the membrane potential and the slow ionic variable, respectively. q is a variable that compose negative feedback current I_f. I_a and I_c are constant bias currents. I_{stim} is a stimulus current given externally. C_y, C_n, and C_q are time constants for variables y, n, and q, respectively. $g_y(y)$, $f_m(y)$, $f_n(y)$, and $f_p(y)$ are hypertangent functions.

$$g_y(y) = S_y \frac{1 - exp(-\frac{\kappa}{U_T}(y-\theta_y)/2)}{1 + exp(-\frac{\kappa}{U_T}(y-\theta_y)/2)}, \quad (5)$$

$$f_x(y) = M_x \frac{1}{1 + exp(-\frac{\kappa}{U_T}(y-\delta_x))}, \quad (6)$$

where $x = m$, n, and p. κ and U_T are capacitive coupling ratio and thermal voltage, respectively. S_y, M_x, θ_y, and δ_x are constants that are determined by voltages applied externally. These functions are implemented easily by differential pair circuitry.

By selecting appropriate parameter values, these equations can produce the mathematical structure described in the previous section.

Equations (1) and (2) comprise basic excitable system, which can reproduce the same mathematical structures as many non-bursting neuron models such as Hodgkin-Huxley and Morris-Lecar equations when $I_f = 0$. In Fig. 1, a phase plane of out basic excitable system when $I_{stim} = 0$ is shown. There are three equilibriums (S), (T), and (U); stable, saddle, and unstable ones, respectively. Both branches of the unstable manifold for (T) reach (S). When we apply and increase sustained current I_{stim}, the longer branch merges with the longer one of the stable manifold for (T) and produces a homoclinic orbit that connects (T) to itself, and finally turns to a stable limit cycle with arbitrarily low frequency (saddle-loop homoclinic orbit bifurcation). This scenario can be overviewed in the bifurcation diagram shown in Fig. 2. We can find bistability between

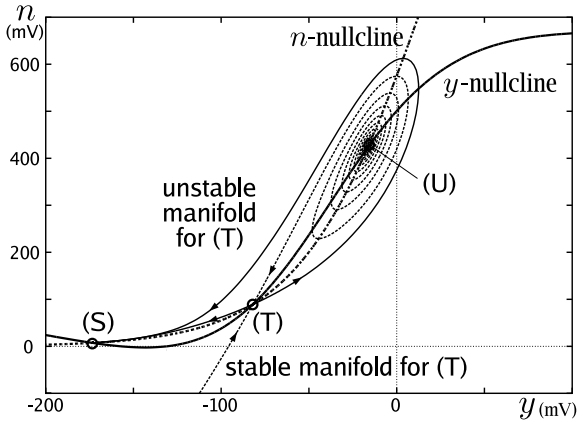

Figure 1: Phase plane of our basic excitable system when I_{stim}=0. (S), (T), and (U) are stable, saddle, and unstable points, respectively. Both branches of the unstable manifold for (T) end at (S).

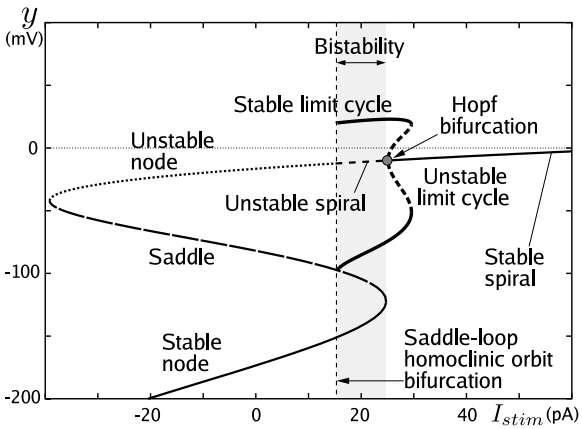

Figure 2: Bifurcation diagram of our basic excitable system ($I_f = 0$). A stable limit cycle emerges via saddle-loop homoclinic orbit bifurcation at I_{stim} = 15.5 pA. It has arbitrarily low frequency.

a stable limit cycle and a stable node in the gray area in the figure.

Equations (3) and (4) comprise negative feedback system that generates current I_f that increases while membrane potential y is low, decreases while y is high. It operates as a dynamical stimulus current applied to the basic excitable system that allows the system to generate burst firing patterns as shown in Fig. 3. When the system is at resting state (stable node), y is low and I_f increases till the resting state vanishes via saddle-node bifurcation. Then the system jumps to the stable limit cycle that is the only stable state. This means the system fires repetitively. Because y is high in this orbit, I_f decreases till the orbit vanishes via saddle-loop homoclinic orbit bifurcation. Then the system jumps to the resting state and stops firing. We show a time series example of y in Fig. 4. It has square-like firing phase.

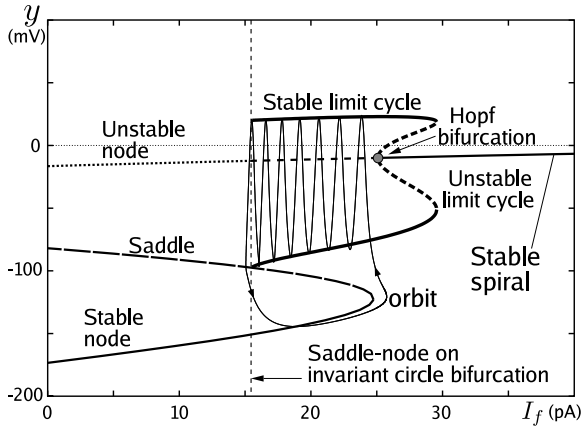

Figure 3: Mechanism of burst firing in our silicon neuron model illustrated in a bifurcation diagram. The horizontal axis (bifurcation parameter) is I_f, which functions as a dynamical stimulus current. Thus, we obtain the same bifurcation diagram as shown in Fig. 2.

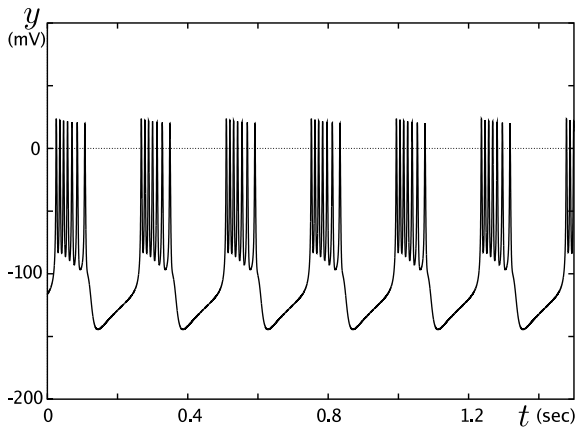

Figure 4: Burst firing patterns observed in simulation of the system described in (1)–(6).

Our system equations are able to be implemented by a circuit whose block diagram is shown in Fig. 5.

They are composed of differential pair, current mirror, and current-mode integrator circuits. Blocks of $f_x(y)$ where $x = m$, n, and p and current mirrors are realized by simple circuit whose schematic is as in Fig. 6(a). M_x and δ_x are configured by the voltages applied at terminals V_M and V_δ, respectively. The other terminals are connected to y line in the block diagram. Figure 6(b) is schematic of $g_y(y)$ block. Differential pair circuitry in this block contains source-degenerated FETs, which realize denominator of 2 in the exponential terms in eq. (5). S_y and θ_y are configured by the voltages applied at terminals V_S and V_θ, respectively. The other terminals are connected to y line in the block diagram. The aspect ratio of the FETs in these circuits is $4\mu/16\mu$ for M1, $2\mu/8\mu$ for M2, M3, M4, and M5, and $2\mu/2\mu$ for M6 and M7. Both of the current mirrors are cascaded.

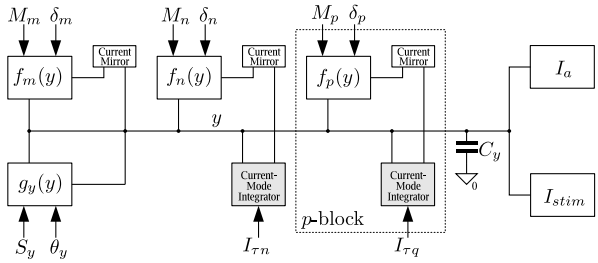

Figure 5: Block diagram of our silicon neuron.

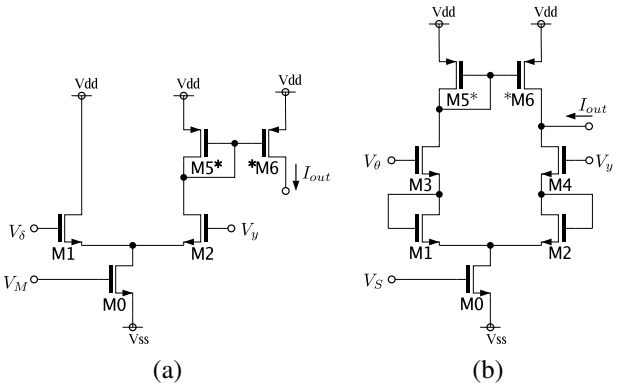

Figure 6: Schematic of differential pair circuits utilized in our silicon neuron. (a) Circuit for $f_x(y)$ and current mirror blocks in Fig. 5. (b) Circuit for $g_y(y)$ block. M_x, δ_x, S_y, and θ_y are applied at V_M, V_δ, V_S, and V_θ. The other terminals are connected to line y in the block diagram. Current mirrors are cascaded.

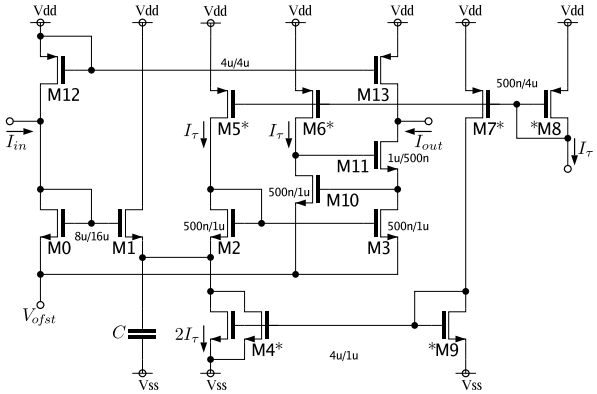

Figure 7: Schematic of our current-mode integrator. I_{out} is temporal integration of $I_{in} - I_{out}$. The time constant depends on C and I_τ. V_{ofst} is connected to constant voltage source, which shifts the gate voltage of M0, M1, M2, and M3 up sufficiently to allow M4 and M9 operate appropriately.

We show a schematic of our current-mode integrator circuit in Fig. 7. It is similar to one in [1], but tuned to be

suitable for implementation by relatively fine process such as .35μ. The aspect ratio of the FETs is 8μ/16μ for M0 and M1, 500n/1μ for M2, M3, and M10, 4μ/1μ for M4 and M9, 500n/4μ for M5, M6, M7, and M8, 1μ/500n for M11, and 4μ/4μ for M12 and M13. Current mirrors composed of M4 and M9 and M5, M6, M7, and M8 are cascaded. The equation of this circuit is

$$\frac{dI_{out}}{dt} = \frac{I_\tau}{CU_T}(I_{in} - I_{out}), \tag{7}$$

where C is capacitance of the capacitor in the circuit. The time constant depends on I_τ. Differential equations of variables n and q (eqs. (2) and (3)) is solved by this circuit, where the first one is by capacitor C_y. The capacitance is 4.5 pF for C_y and 5 pF and 25 pF for Cs in current-mode integrator blocks for n and q, respectively.

We performed simulation of our silicon neuron circuit utilizing HSPICE simulator with technology library of TSMC .35μ mixed signal process. We obtained burst firing time series with a parameter setting similar to that used in numerical simulation shown in Figs. 3 and 4. We show an example of the time series in Fig. 8. The period of burst is roughly 600 msec.

There are slower burst neurons in nerve system whose periods are longer than several seconds. If we are to reproduce such neurons in silicon, C have to be larger or I_τ have to be lower in the current-mode integrator block for variable q. This is because the time constant of variable q dominates the period of burst firing. Though, capacitance of 25 pF requires 28800 μm^2, which is almost limit of fabrication and I_τ is 6.45 pA, which is not realistic to decrease. To realize slower burst firing, we have to explore improvement of system equations and adoption of process that allows larger capacitance.

We designed mask layout shown in Fig.9 and submitted it to fabrication by TSMC .35μ mixed signal process.

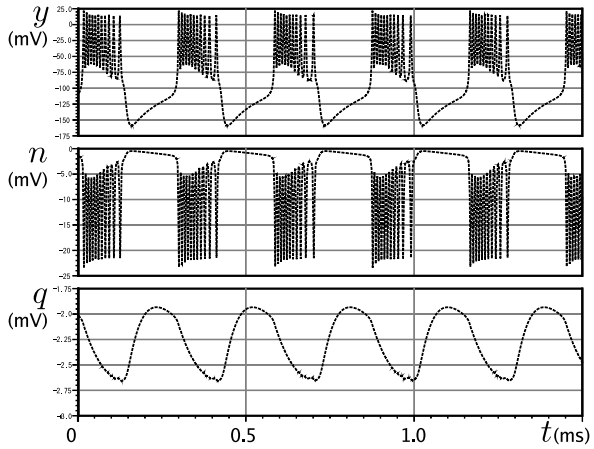

Figure 8: Burst firing time series observed in simulation of our silicon neuron circuit. (HSPICE simulator with technology library of TSMC .35μ mixed signal process)

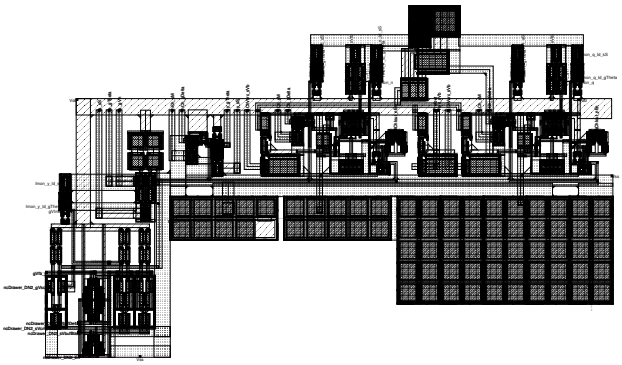

Figure 9: Mask layout of our silicon neuron circuit designed for fabrication by TSMC .35μ mixed signal process.

Acknowledgments

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