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Application of Latency Insertion Method to CMOS Circuit Simulation

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Abstract—This paper describes one of the accurate application techniques of Latency Insertion Method to a CMOS circuit simulation. First, the update equations of a CMOS inverter are formulated for 3 regions. Then, we discuss the accuracy of the proposed technique and the existing one with some actual numerical results. Finally, it is confirmed that the proposed technique enables more accurate and faster simulation of a CMOS inverter chain circuit than an existing one.

1. Introduction

With the rapid progress of circuit integration technologies, high-speed and high-density electronic circuits have been designed. Then, a variety of effects on the plane and the interconnects such as signal delay, reflection, crosstalk, and simultaneous switching noise (SSN) which is induced by the voltage fluctuations on the power/ground planes, lead to unexpected errors on circuits. Therefore, it becomes important to verify the electronic circuit behaviors including these effects at the early stage of circuit design flow.

From a circuit simulation point of view, a net-list, which is mainly provided by an extractor that extracts circuit element parameters from the object to be analyzed and outputs them as net-lists, includes an enormous number of parasitic elements in order to verify the exact behaviors of the chips and packages. In addition, the nonlinear circuit elements such as MOSFETs have to be also simulated. These facts cause the large amount of time consuming task for a SPICE-like simulator based on the matrix solver. Therefore, fast simulation method different from SPICE-like ones are strongly demanded. Our recent researches indicate that Latency Insertion Method in [1] can be one of noticeable methods for a fast simulation of large linear networks [3].

As mentioned above, for SPICE-like simulators, the transient analysis including a number of nonlinear circuit elements becomes a very time consuming task because of the calculations for the Jacobian matrix at every time point. Although there exists the technique that applies Latency Insertion Method to a CMOS inverter circuit and enables to do the fast simulation [2], the accuracy is not always comfortable because of its rough modeling of a CMOS inverter. In this paper, we describe an improved technique which is more accurate one to apply Latency Insertion Method to a CMOS inverter circuit using the detailed modeling of it. It is indicated that the proposed technique enables to do the more accurate simulation compared with the existing one.

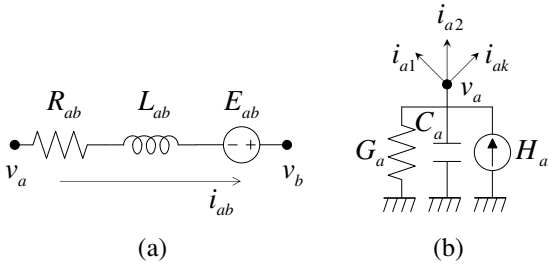

Figure 1: (a) Branch topology for LIM. (b) Node topology for LIM.

2. Latency Insertion Method (LIM)

In this section, we describe the Latency Insertion Method (LIM) which is the fast circuit simulation technique proposed in [1]. In common circuit simulation algorithms, the currents and voltages are updated at the same time by calculating a circuit equation. In the LIM algorithm, in contrast, the current and voltage variables are collocated in half time steps and then all of the branch currents and the node voltages are calculated in turn as time progresses. In order to generate the updating formulas for LIM, a topology of the network has to meet the following requirements: Each branch in the network must contain an inductance as shown in Fig. 1(a) and each node in the network must provide a capacitive path to the ground as shown in Fig. 1(b). Otherwise, a small inductor is inserted into the branch and a small shunt capacitor is added to the corresponding node respectively.

By applying Kirchhoff's voltage low (KVL) to the branch shown in Fig. 1(a) and solving the equation for the unknown current lead to

$$i_{ab}^{n+1} = i_{ab}^{n} + \frac{\Delta t}{L_{ab}} \left(v_a^{n+\frac{1}{2}} - v_b^{n+\frac{1}{2}} - R_{ab} i_{ab}^{n} + E_{ab}^{n+\frac{1}{2}} \right), \quad (1)$$

where $E_{ab}^{n+\frac{1}{2}}$ is the voltage source. By applying Kirchhoff's current low (KCL) to the node shown in Fig. 1(b) and solv-

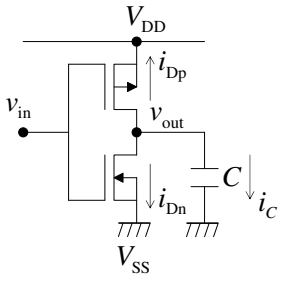

Figure 2: CMOS inverter with a load capacitor.

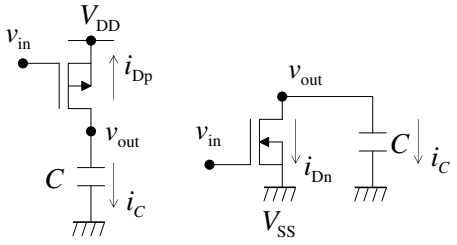

Figure 3: Two separated states of CMOS inverter in Fig. 2: (a) High to Low transition. (b) Low to High transition.

ing the equation for the unknown voltage lead to

$$v_a^{n+\frac{1}{2}} = \left(\frac{\Delta t}{C_a + \Delta t G_a}\right)\left(\frac{C_a}{\Delta t} v_a^{n-\frac{1}{2}} + H_a^n - \sum_{k=1}^{M_a} i_{ak}^n\right), \qquad (2)$$

where H_a^n is the current source. By this formulation, the calculation amount is proportional to a sum of the number of branches and nodes. Therefore, the LIM algorithm can reduce the calculation costs of the transient simulation compared to the methods based on the SPICE-like algorithm that needs the matrix solver.

3. Existing Technique for Application of LIM to CMOS Inverter

When verifying a behavior of the latest LSI which propagates high-speed switching signals, it is necessary to analyze the large-scale nonlinear circuit including the MOSFET characteristics. Although there are various MOSFET models which attempt to describe an ideal behavior of the MOSFET, the Shichman-Hodges model is useful for the fast circuit simulation because of its simple description; therefore it is easy to deal with and can be applied to the analysis technique without appreciable complexity.

The Shichman-Hodges model describes the drain current flowing through PMOS and NMOS as the equations which are divided into the three different regions, namely, cutoff, Ohmic and saturation regions. In fact, the drain current flowing through PMOS, i_{Dp}, is written as

$$i_{Dp} = 0 \qquad (3)$$
$$(\, v_{GS} > v_{Tp} \,) \quad \text{(cutoff)},$$

$$i_{Dp} = -\frac{K_p W_p}{L_p}\left(v_{GS} - v_{Tp} - \frac{v_{DS}}{2}\right) v_{DS} \qquad (4)$$
$$(\, v_{GS} \le v_{Tp}, v_{DS} > v_{GS} - v_{Tp} \,) \quad \text{(Ohmic)},$$

$$i_{Dp} = -\frac{K_p W_p}{2L_p}(v_{GS} - v_{Tp})^2 \qquad (5)$$
$$(\, v_{GS} \le v_{Tp}, v_{DS} \le v_{GS} - v_{Tp} \,) \quad \text{(saturation)},$$

and one flowing through NMOS, i_{Dn}, is written as

$$i_{Dn} = 0 \qquad (6)$$
$$(\, v_{GS} < v_{Tn} \,) \quad \text{(cutoff)},$$

$$i_{Dn} = \frac{K_n W_n}{L_n}\left(v_{GS} - v_{Tn} - \frac{v_{DS}}{2}\right) v_{DS} \qquad (7)$$
$$(\, v_{GS} \ge v_{Tn}, v_{DS} < v_{GS} - v_{Tn} \,) \quad \text{(Ohmic)},$$

$$i_{Dn} = \frac{K_n W_n}{2L_n}(v_{GS} - v_{Tn})^2 \qquad (8)$$
$$(v_{GS} \ge v_{Tn}, v_{DS} \ge v_{GS} - v_{Tn}) \quad \text{(saturation)},$$

where $K_{p,n}$, $W_{p,n}$ and $L_{p,n}$ are the transconductance, the channel width and the channel length, respectively. v_{GS}, v_{DS} and $v_{Tp,Tn}$ are the gate-source voltage, the drain-source voltage and the threshold voltage, respectively.

In [2], the LIM algorithm is applied to a CMOS inverter circuit shown in Fig. 2, using the Shichman-Hodges model. The technique in [2] supposes that the behaviors of a CMOS inverter are separated into the two states, namely, high to low transition and low to high transition of the gate voltage as shown in Fig. 3(a) and Fig. 3(b). In other words, the high to low transition, for example, means the case that if the input voltage of an inverter seems to be low (logical-zero), then, PMOS is turned on and NMOS is turned off so that the output voltage is to be high (logical-one), and therefore, there exist only PMOS and a load capacitor in the circuit. In order to derive the updating formula for the output voltage, v_{out}, for the high to low transition, KCL is applied to the output node of the inverter, thereby the KCL equation can be written as

$$i_{Dp} + i_C = 0, \qquad (9)$$

where

$$i_C = C\frac{dv_{out}}{dt}$$

is the current flowing through the load capacitor in Fig. 3(a). In the case that PMOS is in the cutoff region, substituting (3) into (9) is followed by using the finite difference method, and then, solving the equation for the unknown variable $v_{out}^{n+\frac{1}{2}}$ lead to

$$v_{out}^{n+\frac{1}{2}} = v_{out}^{n-\frac{1}{2}}. \qquad (10)$$

Eq. (10) means that the output voltage does not change before and after updating. Next, in the case that PMOS is in the Ohmic region, substituting (4) into (9) with consideration for $v_{GS} = v_{in} - V_{DD}$ and $v_{DS} = v_{out} - V_{DD}$ from Fig. 3(a) and using the finite difference method lead to

$$-\frac{K_p W_p}{L_p}\left(v_{in}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}} - v_{Tp} - \frac{v_{out}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}}}{2}\right)\left(v_{out}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}}\right)$$
$$+C\frac{v_{out}^{n+\frac{1}{2}} - v_{out}^{n-\frac{1}{2}}}{\Delta t} = 0, \quad (11)$$

where $V_{DD}^{n+\frac{1}{2}}$ is the supply voltage for the inverter and the source voltage for PMOS. Then, combining like terms related to the unknown variable $v_{out}^{n+\frac{1}{2}}$ to simplify the equation leads to

$$a_p\left(v_{out}^{n+\frac{1}{2}}\right)^2 + b_p v_{out}^{n+\frac{1}{2}} + c_p = 0, \quad (12)$$

where

$$\begin{aligned} a_p &= \frac{\alpha_p}{2}, \\ b_p &= -\alpha_p\left(v_{in}^{n+\frac{1}{2}} - v_{Tp}\right) + 1, \\ c_p &= \alpha_p\left(v_{in}^{n+\frac{1}{2}} - \frac{v_{DD}^{n+\frac{1}{2}}}{2} - v_{Tp}\right)v_{DD}^{n+\frac{1}{2}} - v_{out}^{n-\frac{1}{2}} \end{aligned}$$

and

$$\alpha_p = \frac{K_p W_p \Delta t}{L_p C}$$

are the constants at $(n+1/2)$-th time point. Because (12) is a quadratic equation, solving it using the quadratic formula leads to

$$v_{out}^{n+\frac{1}{2}} = \frac{-b_p + \sqrt{b_p^2 - 4a_p c_p}}{2a_p}. \quad (13)$$

On the other hand, in the case of the saturation region, substituting (5) into (9) and using the finite difference method lead to

$$-\frac{K_p W_p}{2L_p}\left(v_{in}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}} - v_{Tp}\right)^2 + C\frac{v_{out}^{n+\frac{1}{2}} - v_{out}^{n-\frac{1}{2}}}{\Delta t} = 0. \quad (14)$$

Then, solving (14) for the unknown variable $v_{out}^{n+\frac{1}{2}}$ leads to

$$v_{out}^{n+\frac{1}{2}} = \frac{\alpha_p}{2}\left(v_{in}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}} - v_{Tp}\right)^2 + v_{out}^{n-\frac{1}{2}}. \quad (15)$$

The right-hand side of (10), (14) and (15) are constants at $(n+1/2)$-th time point, and therefore, only assignment operations are required to update the output voltage. Eqs. (10), (13) and (15) are the updating formulas for the output voltage for high to low transition in the case that PMOS is in cutoff, Ohmic and saturation regions, respectively. The updating formulas for the low to high transition, where NMOS is turned on as shown in Fig. 3(b), can be derived in a similar way.

Table 1: Five states for CMOS inverter.

states	PMOS	NMOS
(I)	Ohmic	cutoff
(II)	Ohmic	saturation
(III)	saturation	saturation
(IV)	saturation	Ohmic
(V)	cutoff	Ohmic

Although the existing technique achieves the application of the LIM algorithm to a CMOS inverter circuit, the model seems to be slightly rough because each one of the two states includes only an unilateral MOSFET, namely PMOS or NMOS. Consequently, it also seems that the accuracy of the existing model may not be unfit for the exact simulation of the circuit which includes a number of MOSFETs. In the next section, we propose the more accurate application technique of LIM to a CMOS inverter circuit.

4. Proposed Technique for CMOS Inverter

Our technique is different from the existing one in the state definition of a CMOS inverter. The behavior of a CMOS inverter indicates that if the input voltage changes from low to high, the output voltage should change from high to low concurrently. Thus, we assume that the state of a CMOS inverter changes through the five states, from (I) to (V) as shown in Table 1, as the input voltage changes from low to high. These five states describe the natural transitions of a CMOS inverter because PMOS changes in the order corresponding to Ohmic, saturation and cutoff regions and NMOS changes in reverse of it, and 5 combinational cases, shown in Table 1, which are constituted by the three regions of the MOSFET, are considered.

The KCL equation for the output node of the CMOS inverter in Fig. 2 can be written as

$$i_{Dp} + i_{Dn} + i_C = 0. \quad (16)$$

And then, the each drain current equation, (3)-(8), is substituted to (16) for each state of a CMOS inverter as shown in Table 1. For example, in the case of the state (II) which means that PMOS is in Ohmic region and NMOS is in saturation region, substituting (4) and (8) to (16) including $V_{SS} = 0$ and using the finite difference method lead to

$$-\frac{K_p W_p}{L_p}\left(v_{in}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}} - v_{Tp} - \frac{v_{out}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}}}{2}\right)\left(v_{out}^{n+\frac{1}{2}} - V_{DD}^{n+\frac{1}{2}}\right)$$
$$+\frac{K_n W_n}{2L_n}\left(v_{in}^{n+\frac{1}{2}} - v_{Tn}\right)^2 + C\frac{v_{out}^{n+\frac{1}{2}} - v_{out}^{n-\frac{1}{2}}}{\Delta t} = 0. \quad (17)$$

Then, combining like terms related to the unknown variable $v_{out}^{n+\frac{1}{2}}$ and using the quadric formula lead to the updating formula which has the same form as (13). In a similar manner,

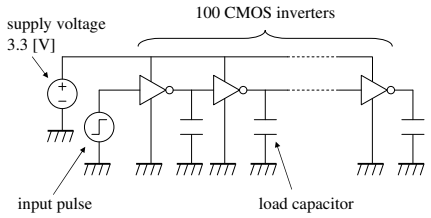

Figure 4: CMOS inverter chain circuit.

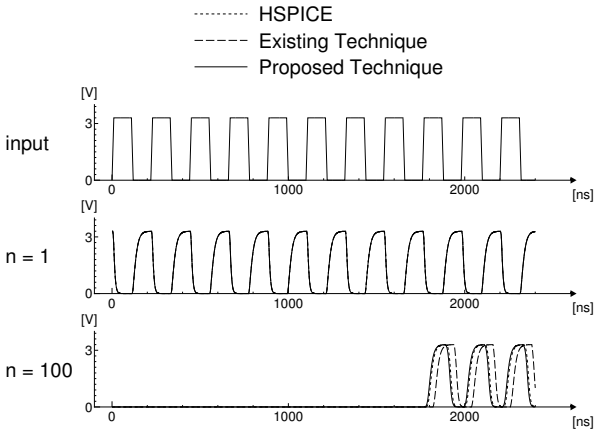

Figure 5: Waveform results for a CMOS inverter chain circuit.

the all updating formulas, which depend on the states in Table 1, can be derived and written as

$$v_{\rm out}^{n+\frac{1}{2}} = \frac{-b_{\rm I} + \sqrt{b_{\rm I}^2 - 4a_{\rm I}c_{\rm I}}}{2a_{\rm I}}, \quad (18)$$

$$v_{\rm out}^{n+\frac{1}{2}} = \frac{-b_{\rm II} + \sqrt{b_{\rm II}^2 - 4a_{\rm II}c_{\rm II}}}{2a_{\rm II}}, \quad (19)$$

$$v_{\rm out}^{n+\frac{1}{2}} = \frac{\alpha_{\rm p}}{2}\left(v_{\rm in}^{n+\frac{1}{2}} - v_{\rm DD}^{n+\frac{1}{2}} - v_{\rm Tp}\right)^2 - \frac{\alpha_{\rm n}}{2}\left(v_{\rm in}^{n+\frac{1}{2}} - v_{\rm Tn}\right)^2 + v_{\rm out}^{n-\frac{1}{2}}, \quad (20)$$

$$v_{\rm out}^{n+\frac{1}{2}} = \frac{-b_{\rm IV} + \sqrt{b_{\rm IV}^2 - 4a_{\rm IV}c_{\rm IV}}}{2a_{\rm IV}}, \quad (21)$$

$$v_{\rm out}^{n+\frac{1}{2}} = \frac{-b_{\rm V} + \sqrt{b_{\rm V}^2 - 4a_{\rm V}c_{\rm V}}}{2a_{\rm V}}, \quad (22)$$

where $a_{\rm I\text{-}V}$, $b_{\rm I\text{-}V}$ and $c_{\rm I\text{-}V}$ are the constants. Eqs. (18)-(22) correspond to the updating formulas based on the five states (I)-(V), respectively. The modeling using the five states of a CMOS inverter can be useful as more detailed model than the existing one and it is expected that a more accurate simulation can be done.

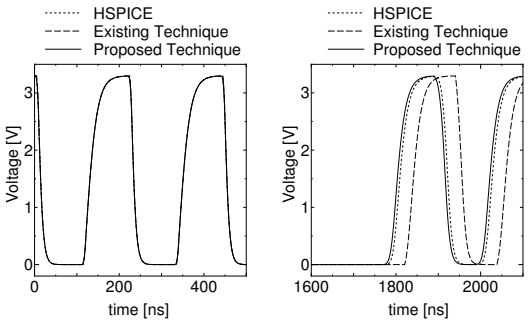

Figure 6: Detailed waveform results. (a) Output voltage from first inverter. (b) Output voltage from 100th inverter.

5. Numerical Results

Fig. 4 shows a CMOS inverter chain circuit which consists of 100 series-connected CMOS inverters with load capacitors, 3.3 V supply voltage and pulse signal generator. We use this example circuit for the verification of each technique.

In order to verify the accuracy of each technique, the waveform results for the example circuit are shown in Fig. 5. "input" of Fig. 5 means the waveform of the input pulse for the first inverter, and "n = 1" and "n = 100" are the output voltages of the first and 100th inverter, respectively. The detailed waveforms of the output voltages from the first and 100th inverters are shown in Fig. 6(a) and Fig. 6(b). These waveform results show that the proposed technique is more accurate than the existing one.

6. Conclusions

In this paper, the one of accurate application techniques of LIM to a CMOS circuit simulation has been described. The existing technique has adopted a slightly rough model for a CMOS inverter, namely high to low transition and low to high transition, thereby the accuracy of it is not comfortable. We have proposed the way how to perform more accurate modeling for a CMOS inverter and apply the LIM algorithm to it. As a result, we have confirmed that the proposed technique can analyze a CMOS inverter chain circuit more accurately than the existing one.

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