

Subthreshold CMOS Bistable Circuit for Stochastic Memory Device

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Abstract—We propose a bistable circuit and a parallel shift circuit to realize a stochastic memory, which can store the probability of an output random number sequence. The bistable circuit forms a double-well potential using the subthreshold characteristics of metal-oxide-semiconductor field-effect transistors(MOSFETs), and the output voltage is stabilized at two values. The parallel shift circuit shifts the potential left and right in parallel by the gate voltage of the floating-gate MOSFET. Simulation Program with Integrated Circuit Emphasis(SPICE) reveal that adding noise to the proposed circuit results in a random output voltage stability. Furthermore, the output voltage stability probability is found to vary with the value of the floating gate voltage.

1. Introduction

With the advances in the Internet of Things in recent years, edge computing is attracting increasing attention, and the edge devices that comprise it are required to have a small circuit area and low-power-consumption circuit configuration owing to their applications. **Stochastic computing (SC)** [1] is expected to reduce the area and power consumption of arithmetic circuits, such as the ability to calculate multiplications with a single AND gate, using probabilities represented by bit strings. Therefore, SC is considered very useful for applications that require parallel processing of simple sum-of-products operations, such as neural networks. However, although various architectures have been proposed in previous studies [2–4], conventional memory circuits cannot directly store the probabilities represented by bit strings; thus, memory utilization issues exist, and the method has not progressed to a practical stage.

In this study, we attempted to realize SC architecture, which has been difficult to implement in hardware, by realizing stochastic memory that can directly store probabilities. Furthermore, by utilizing the subthreshold character-

istics of metal-oxide-semiconductor field-effect transistors (MOSFETs), the circuit’s power consumption can be further reduced. This study describes a stochastic memory based on the bistable system model and then proposes a bistable circuit using subthreshold complementary metal-oxide-semiconductor(CMOS). Next, we present the results of the simulation of a stochastic memory operation using a parallel shift circuit with floating-gate MOSFETs.

2. SC and Neural Networks

SC performs calculations using bit strings represented by logical “1” and “0” binary values. For example, to handle E represented by n bits in SC, it must be converted into a bit sequence using a uniform random number R_i (encoding). Conversely, to represent a bit sequence used in SC as an n -bit binary number, a counter should be used (decode).

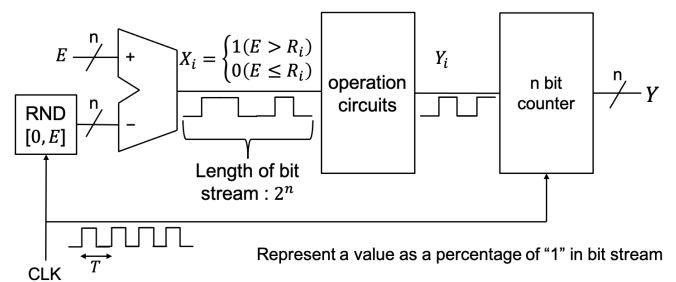







Figure 1: Outline of SC [4]

Updating weights by backpropagation is very important for neural networks, and a large memory is essential for this. However, as mentioned above, SC requires a conversion circuit, which causes a large cost for the use of memory. Thus, SC can be configured with low-cost arithmetic circuits, whereas memory circuits require encoders and decoders, which is a hindrance in achieving lower circuit area and power consumption.

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3. Overview of the proposed circuit

3.1. Stochastic memory based on bistable systems

For the case where noise is added to x_0 , an unstable state is generated, and the system moves to x_1, x_2 in an attempt to become stable. If this is repeated periodically, a sequence of random numbers can be obtained as an output. For such a case, a parallel shift of the potential should be considered, for example, moving the potential to the left creates a barrier on the x_1 side. This increases the probability of stability at x_2 and decreases the probability of stability at x_1 . Thus, the probability taken by the output random number sequence can be changed by translating the potential to the left or right.

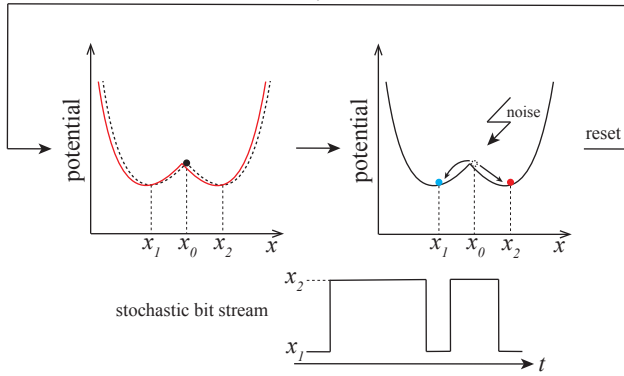


Figure 2: probability change due to the parallel shift of potentials

Therefore, by combining a circuit that forms a bistable system and a circuit that translates the potential, a circuit that outputs a random number sequence with an arbitrary probability can be constructed. Furthermore, if the amount of the potential parallel shift can be stored in memory, a random number sequence with a probability corresponding to the written value will be output, and probabilistic memory will be realized.

3.2. Circuit equations and potentials

The proposed circuit consists of a bistable circuit and a parallel shift circuit, with a positive power supply V_{DD} , a negative power supply V_{SS} and ground as power supplies. Initially, the output voltage V_{out} is set to 0 V; this value changes as the capacitor charges and discharges owing to the output current of the bistable circuit. The circuit equation of the bistable circuit is given in Eq.(1) and the parallel shift circuit is given in Eq.(2); additionally, all MOSFETs operate in the subthreshold region.

$$C_{out} \frac{dV_{out}}{dt} = (I_{na} - I_{nb}) + (I_{pb} - I_{pa}) \quad (1)$$

$$V'_{out} \approx V_{out} - \frac{1}{4}(V_{DD} - V_{fg}) \quad (2)$$

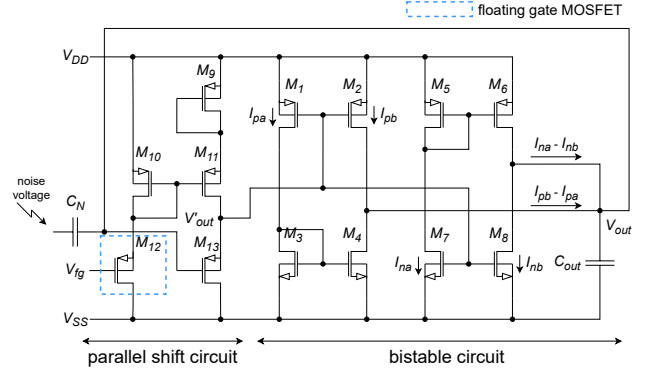


Figure 3: subthreshold CMOS bistable circuit

For MOSFETs in the subthreshold region, the drain current varies as an exponential function of the gate voltage V_g . The drain currents I_n and I_p of NMOS and PMOS in the saturation region are expressed by Eq.(3) and Eq.(4) [5] using the gate voltage V_g , source voltage V_s , substrate voltage V_b , and thermal voltage U_T , respectively. Here, I_{n0} and I_{p0} are the zero bias currents, and κ_n and κ_p are the capacitive coupling ratios from gate to channel.

$$I_n = I_{n0} e^{\{\kappa_n(V_g - V_b) - (V_s - V_b)\}/U_T} \quad (3)$$

$$I_p = I_{p0} e^{\{\kappa_p(V_b - V_g) - (V_b - V_s)\}/U_T} \quad (4)$$

Assuming that the MOSFET parameters $M_1, M_2, M_7,$ and M_8 in the figure are $I_{a0}, \kappa_a, I_{b0},$ and κ_b , respectively, $I_{na}, I_{nb}, I_{pa},$ and I_{pb} are expressed using Eq.(5).

$$\begin{aligned} I_{na} &= I_{a0} e^{\kappa_a(V'_{out} + V_{DD})/U_T} \\ I_{nb} &= I_{b0} e^{\kappa_b(V'_{out} + V_{DD})/U_T} \\ I_{pa} &= I_{a0} e^{\kappa_a(V_{DD} - V'_{out})/U_T} \\ I_{pb} &= I_{b0} e^{\kappa_b(V_{DD} - V'_{out})/U_T} \end{aligned} \quad (5)$$

For the potential function H to be bistable, a relationship such as that in Eq.(6) is required with respect to V_{out} .

$$\frac{\partial H}{\partial t} = \frac{\partial H}{\partial V_{out}} \frac{dV_{out}}{dt} < 0 \quad (6)$$

This gives $\frac{\partial H}{\partial V_{out}} = -\frac{dV_{out}}{dt}$, where H can be obtained by substituting Eq.(1) and integrating with V_{out} .

$$H = \frac{U_T}{C_{out}} \left\{ \frac{I_{b0} e^{\kappa_b V_{DD}/U_T}}{\kappa_b} (e^{\kappa_b V'_{out}/U_T} + e^{-\kappa_b V'_{out}/U_T}) - \frac{I_{a0} e^{\kappa_a V_{DD}/U_T}}{\kappa_a} (e^{\kappa_a V'_{out}/U_T} + e^{-\kappa_a V'_{out}/U_T}) \right\} \quad (7)$$

For this equation, a double-well potential can be obtained by setting $I_{a0}, \kappa_a, I_{b0},$ and κ_b to appropriate values. Owing to constraints on the length of the study, we have omitted details on the relationship between each parameter and the potential.

4. Simulation

To verify the bistable and stochastic behavior of the proposed circuit, simulations were performed using ngspice. A transient noise source that can be handled by ngspice was used for the input noise, and it was set to a period of 1 ms and amplitude of 0.1 V, considering the stability time and the stability voltage width. Additionally, the source was connected to V_{out} by capacitor C_N . Table 1 shows the circuit constants and MOSFET subthreshold constants used in the simulation. Here, M_1 and M_7 are operated with I_{a0} and κ_a ; M_2 and M_8 with I_{b0} and κ_b ; and the rest with I_0 and κ [6]. Substituting the constant values into Eq.(7) yields a double-well potential as shown in Fig.(4).

Table 1: Value of constant

| | | | | | | | |
|----------|---------|----------|---------|------------|-------|-----------|------|
| V_{DD} | 0.25 V | I_0 | 0.72 aA | κ | 0.700 | C_{out} | 1 fF |
| V_{SS} | -0.25 V | I_{a0} | 3.09 aA | κ_a | 0.650 | C_N | 1 fF |
| U_T | 26 mV | I_{b0} | 7.30 aA | κ_b | 0.728 | | |

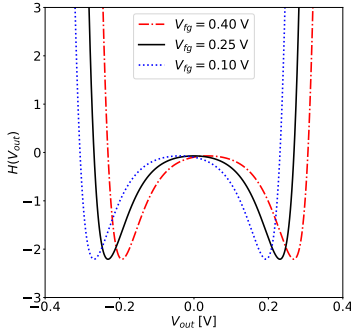


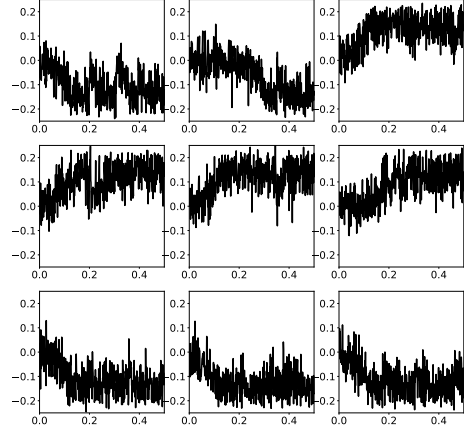
Figure 4: Circuit potentials

4.1. Stochastic stable characteristics

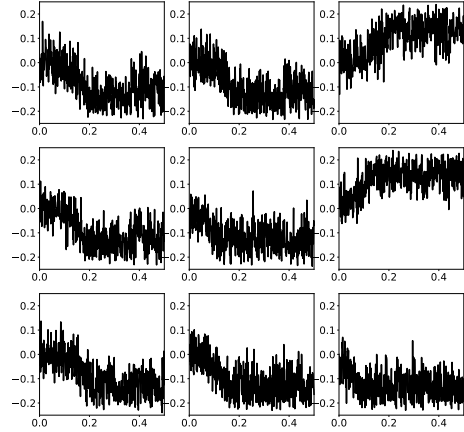
The initial value of V_{out} was set at the center of the potential (0 V) and the transient response was simulated when V_{fg} was varied; nine results are shown in Fig.5. The transient response of V_{out} was found to oscillate around 0 V immediately after starting the analysis; however, after a certain time, it oscillated around ± 0.15 V. This shows that V_{out} was stochastically stabilized by providing noise. With these observed data, the stability probability of V_{out} concerning V_{fg} could be roughly estimated. Note that hereafter, $p(V_{fg})$ is defined as the stability probability as in Eq.(8).

$$p(V_{fg}) = \frac{\text{Number of stable at } V_{out} > 0 \text{ V}}{\text{Number of trials } N} \quad (8)$$

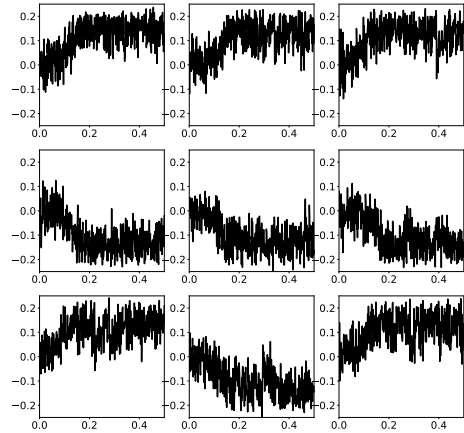
If $N = 9$ based on the results of Fig.(5), the stability probability can be expressed as $p(0.219) = 0.56$, $p(0.229) = 0.44$, and $p(0.239) = 0.22$.



(a) $V_{fg} = 0.229$ V



(b) $V_{fg} = 0.239$ V



(c) $V_{fg} = 0.219$ V

Figure 5: Transient response

4.2. Output probability change characteristics

To confirm the variation characteristics of $p(V_{fg})$ with respect to V_{fg} , V_{fg} was varied in the 0.10 ~ 0.35 V range by 0.02 V, and a stable operation was performed 100 times at each V_{fg} . Based on the results, $p(V_{fg})$ was obtained from Eq.(8). This simulation was performed 10 times under the same conditions, and the results are summarized in Fig.6.

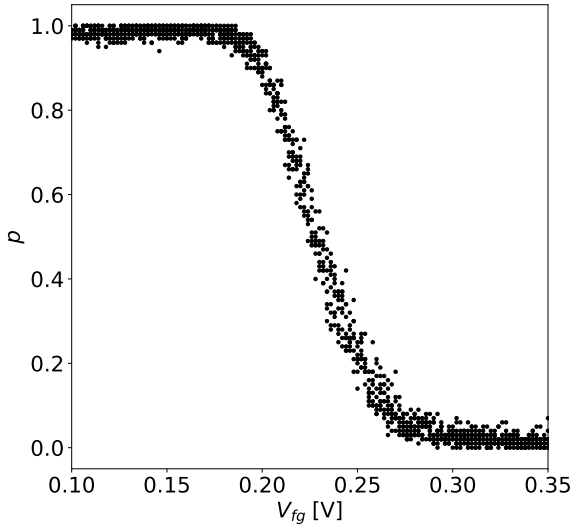


Figure 6: Stability probability

This result revealed that $p(V_{fg})$ could be controlled over the entire range of V_{fg} if V_{fg} was varied between approximately 0.17 ~ 0.27 V. Assuming that the floating gate MOSFET used here can rewrite V_{fg} with 8-bit precision, the minimum change range of V_{fg} will be 2 mV as the supply voltage is 0.5 V this time. Therefore, $p(V_{fg})$ will be divided into approximately 50 parts, and the probability memory of the proposed circuit will have an accuracy of 5 ~ 6 bit.

To calculate the power consumption of the proposed circuit in stable operation, consider the case where linear feedback shift registers are used as M-sequence random numbers as noise sources. If the output of each register is connected to another proposed circuit, the power consumed by the proposed circuit and one flip-flop is the total power consumption. When the MOSFETs used in the flip-flop were the same as in the proposed circuit, the simulation results revealed that the power consumption at stable V_{out} was at most 22.2 fJ. Compared with a true random number generator [7], whose output probability can be varied, its power consumption was less than 1/30; this indicates that a low-power, low-area stochastic memory can be realized in future.

5. Conclusion

Considering a stochastic memory based on a bistable system model, we proposed a double-well potential that utilizes the subthreshold characteristics of MOSFETs. A circuit system was constructed from this potential function, and by using a floating-gate MOSFET, the operation of the circuit to store probabilities was simulated and demonstrated.

However, SC requires a decoder/encoder, which makes the memory circuits huge when the scale of computation becomes large. Therefore, the proposed circuit combines a floating-gate MOSFET, which is an existing memory element, and a bistable circuit using subthreshold CMOS. The study results revealed that the retention of analog voltage values can be used to store probabilities.

Acknowledgments

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