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Toward a Neural Network Computing: A Novel NN-SRAM

Ali M. Haidar*, Nayif Saleh*, Wassim Itani* and Hiroyuki Shirahama†
* Department of Electrical and Computer Engineering
Beirut Arab University, Faculty of Engineering, Beirut 11-5020, Lebanon
† Department of Technology Education, Faculty of Education, Ehime University
3 Bunkyou-chou, Matsuyama 790-8577, Japan
E-mails: ari@bau.edu.lb, nayif.saleh@bau.edu.lb, w.itani@bau.edu.lb, shirahama@ed.ehime-u.ac.jp

***Abstract* — A novel Neural Network Memory cell design is proposed. A Neural Network Static RAM (NN-SRAM) consists of internal latch that stores binary information. The stored information remains valid as long as power is applied to the NN-SRAM. The NN-SRAM is easy to use, where the simulation (using Matlab/Simulink) showed that the read and write cycles are short, reducing the energy consumption, thus it can be used in wireless sensor networks for extending the life time. The NN-SRAM is volatile, but no need to refresh. Also, this paper presents the neural network internal structure of *m-words* with *n-bits* SRAM chip. The chip is a combination of NN-SRAM cells and associated neural networks to select the word, read, write, input, and output; these neural networks are used to control the operation of the *m x n* NN-SRAM chip.**

1. Introduction

Memory is a major component of a digital computer and is present in a large proportion of all digital systems [1-6], such as wireless sensor networks. RAM stores data temporarily, and ROM stores data permanently. This paper introduces a new design of NN-SRAM cell. The NN-SRAM cell is easy to use. The design and the operation of the internal latches that store the binary information of NN-SRAM cell will be introduced and described. The stored binary information remains valid as long as power is applied to the NN-SRAM. The simulation result (using Matlab/Simulink) proved that the read and write cycles are short. The NN-SRAM cell is volatile, but this memory cell does not need any refreshing or refresh circuit. The paper includes the internal structure of NN-SRAM chip of *m*-words with *n*-bits per word, which is consisted of an array of *m x n* binary storage cells and associated neural network circuitry to control the operation that select, read, write, input and output the word.

2. Neural Model

The paper begins by introducing the neuron model. Figure 1 shows a simplified mathematical model of the neuron, the weights modulate the effect of the associated input signals, and the transfer function. The neuron impulse is then computed as the weighted sum of the input signals, transformed by the transfer function.

The mathematical characteristics and the activation function are:

$$Oj = \begin{cases} 1 & if \quad net_j \geq \theta_j \\ 0 & if \quad net_j < \theta_j \end{cases}$$

$$\text{net}_j = \sum X_i \, W_{ij}$$

Where W*ij* is the weight vector, X_i is the input vector; and O_j is the output of the function that tests the net input net_j with the threshold θ_j. This type of artificial neural network is called a linear threshold unit.

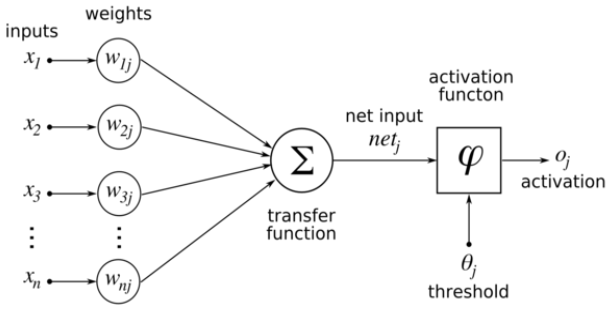

Figure 1. Artificial neuron model

3. Neural Network SRAM

Figure 2 shows the basic structure of the NN-SRAM cell, which is a binary data storage neural network that can be constructed using the basic neuron. The inputs to the NN-SRAM are enabled by a select control signal (S). For Select equal to 0, the stored content is held. For Select equal to 1, the stored content is determined by the values of D (Data Input). The operations are summarized in the truth Table 1. The D input is sampled when S=1; if D is 1, then the Q output goes to 1 placing the NN-SRAM in the set state. If D is 0, then Q goes to 0, placing the NN-SRAM in the reset state.

The NN-SRAM latch receives its designation from its ability to hold data in its internal storage. The binary information present at the data input *D* is transferred to the *Q* output when the control input is enabled; the output *Q* follows changes in the data input, as long as the select control input is enabled. On the other hand, when the select control input is disabled, *the* binary information that is present at input *D* cannot be latched; and the *Q* output will retain its value until the select control input is enabled again. Figure 3 shows the simulation result of the NN-SRAM cell.

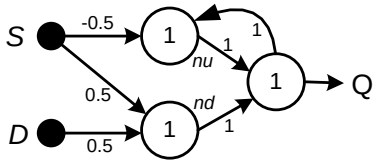

Figure 2. NN-SRAM cell

Table 1: Truth Table for the NN-SRAM

Q	*S*	*D*	*nd*	*nu*	*Next Q*	*Action*	
0	0	0	0	0	0	*hold*	*NC*
1	0	0	0	1	1	*hold*	*NC*
0	0	1	0	0	0	*hold*	*NC*
1	0	1	0	1	1	*hold*	*NC*
0	1	0	0	0	0	*D→Q*	*Reset*
1	1	0	0	0	0	*D→Q*	*Reset*
0	1	1	1	0	1	*D→Q*	*Set*
1	1	1	1	0	1	*D→Q*	*Set*

Figure 4 shows the logic model of the NN-SRAM cell with the associated circuitry to control the operations (Select, Read/Write, and Input/Output). The storage part of the memory cell is the same model as shown in Fig. 2. The inputs to the latch are enabled by a select signal (*S*). For *S*=0, the stored contents is held. For *S* =1, the stored contents is determined by *R'/W* (Read/Write).

To design the controlled NN-SRAM diagrams, the NN-SRAM cell will be controlled by read and write control signal as shown in Fig. 4. The controlled NN-SRAM cell will be used as the main element to form the internal structure of *m x n* NN-SRAM chip, where Fig. 5 shows the structure of *4 x 4* NN-SRAM. The loading of the NN-SRAM cell is now controlled by a Row Select input RS_i. If RS_i = 0, then the cell latch contents remain unchanged. If RS_i = 1, then the values to be loaded into the latches are controlled by data input *D*. In order to change stored value, the read/write signal *R'/*W must be 1 and the selected RS_i must be 1. If data in *D* is 1 the latch is set to 1, and if *D* is 0 the latch is reset to 0, completing the write operation. In order to read stored value, *R'/*W must be 0 and RS_i must be 1. If the stored value is 1, then the output *C* is set to 1; if stored value is 0, then the output *C* is reset to 0, completing the read operation. Table 2 shows the operation for controlled m x n NN-SRAM cell.

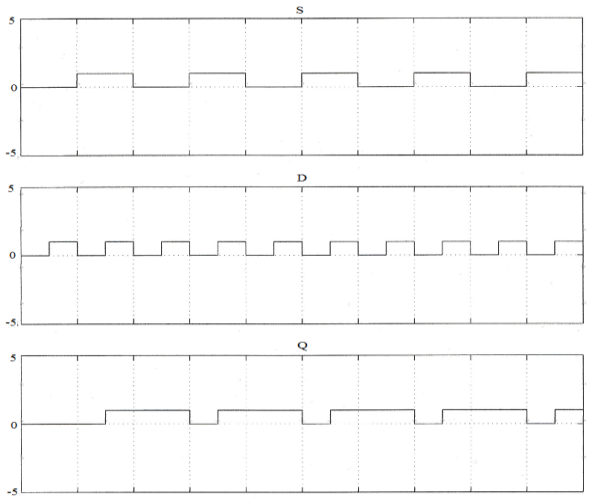

Figure 3. Simulation results for NN SRAM cell.

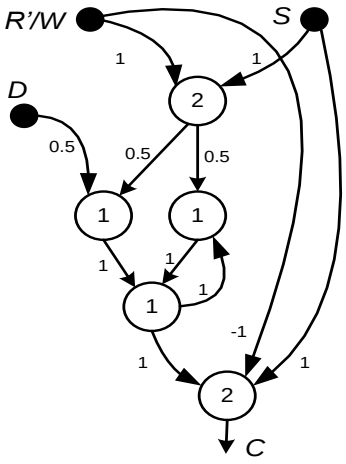

Figure 4. Controlled NN-SRAM cell

Table 2: Truth table for controlled NN-SRAM cell

S	*R'/W*	*Memory Operation*	
0	0	*NC*	*hold*
0	1	*NC*	*hold*
1	0	*Read*	*Q→C*
1	1	*Write*	*D→Q*

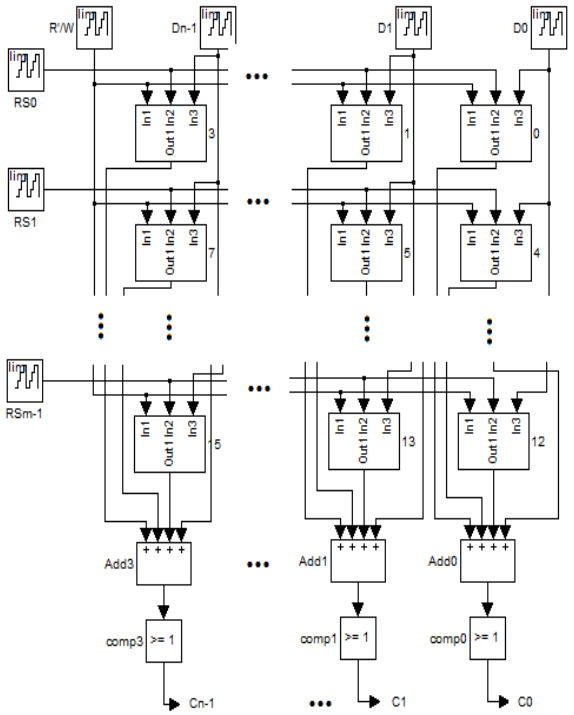

Figure 5: Diagram of a *m x n* SRAM cell array.

Memory chips are usually consisted of SRAM cells plus additional control logic. Figure 5 shows the internal structure of a NN-SRAM chip of *m*-words and *n*-bits per word consists of an array of *m x n* binary NN storage cells and NN associated circuitry. The NN associated circuitry is made up to select the word to be read or written, and to input or output logic. Inside a RAM chip, the decoder with *k* inputs and 2^k outputs is used to control the row select in Fig. 5. Figure 6 shows the *2 x 4* NN decoder, and Table 3 shows the operation.

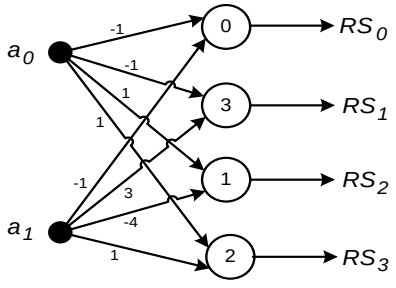

Figure 6. 2 x 4 NN decoder

In order to design a complete m x n NN memory chip, we proposed a 4 x 4 NN SRAM chip of Fig. 7, this is controlled by the decoder of Fig. 6, where the input signals a0 and a1 represent the address, and the output signals RS0, RS1, RS2, and RS3 represent the Row Select used to select the location (word).

Table 3: Truth Table for 2 x 4 decoder

a_0	a_1	RS_0	RS_1	RS_2	RS_3	Active RS_i
0	0	1	0	0	0	RS_0
0	1	0	1	0	0	RS_1
1	0	0	0	1	0	RS_2
1	1	0	0	0	1	RS_3

4. Conclusion

A novel Neural Network Static RAM (NN-SRAM) consists of internal latches that store the binary information was proposed. The NN-SRAM stores binary data and remain valid as long as power is applied. Since the NN-SRAM reduces the energy consumption, it can be used in wireless sensor networks for extending the life time. Finally, this paper presented the structure of 4 x 4 NN-SRAM chips, where the simulation results (using Matlab/Simulink) for this design validate the NN-SRAM functionality.

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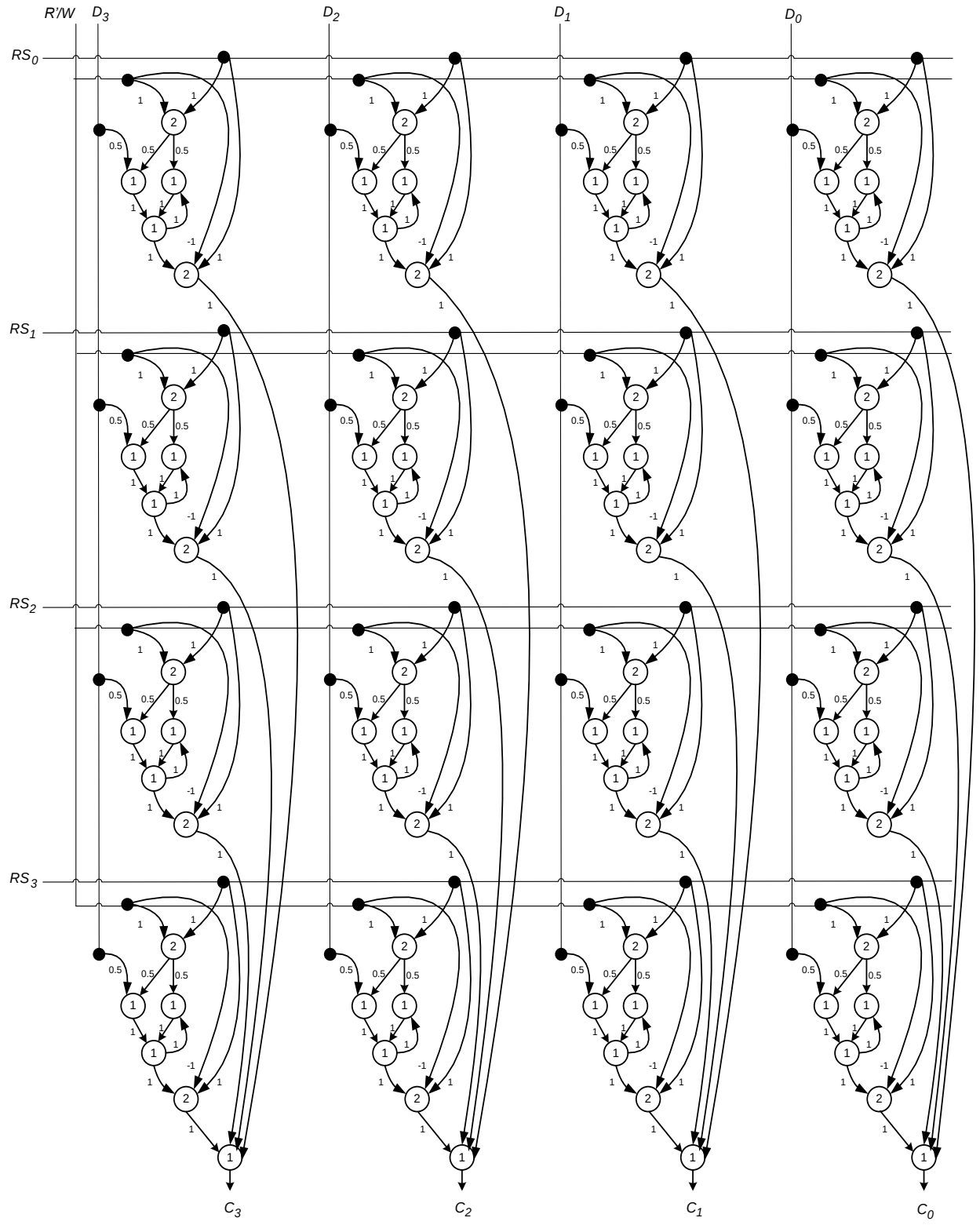

Figure 7: Diagram of *4 x 4* NN-SRAM