Circuit-Based FDTD Method Using Reluctance Matrix

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Abstract— The circuit-based FDTD method for transient analysis of a mutually coupled system, where the inverse inductance, i.e. reluctance matrix is introduced. In an example with the full capacitance and reluctance matrices, we confirm that the proposed method is 23 times faster than HSPICE and 458 times faster than Berkeley SPICE. In the case with the sparse capacitance and reluctance matrices, the proposed method is 69 times faster than HSPICE and 1349 times faster than Berkeley SPICE, whereas a small-scale circuit is analyzed.

I. INTRODUCTION

With rapid progress of VLSI technologies, the designers of VLSI, package, and board have suffered from the signal and power integrity problems. To overcome these problems, routing of VLSI, package, and board are modeled by an RLC network and the transient analysis should be carried out. Recently, a fast simulation technique which is similar to the FDTD method for electromagnetic analysis [1] was proposed [2]. In the FDTD method, electric and magnetic fields are alternately calculated. On the other hand, in the method [2], voltage and current vectors are alternately calculated (we call it the circuit-based FDTD method). It is shown that the circuitbased FDTD method is 100 to 1000 faster than SPICE for the analysis of RLC grid [3]. However, routing of VLSI, package, and board are generally modeled by a mutually coupled system represented by the capacitance and inductance matrices. Therefore, the circuit-based FDTD method is extended to the analysis of a mutually coupled system [3], [4]. However, the inductance matrix is not always obtained. Since the RLC extraction requires a huge computation cost, it is impossible to extract them for the whole area of routing of VLSI, package, and board. Therefore, the RLC values are partially extracted with the window techniques. In this case, the stable inductance matrix is difficult to be extracted with the window technique. Alternatively, the reluctance matrix is extracted [5], [6]. Therefore, the circuit-based FDTD method should be extended to the analysis of a circuit modeled by the reluctance matrix.

In this paper, we present the circuit-based FDTD method for the analysis of a mutually coupled system, where the reluctance matrix is introduced. First, the RLC circuit is expressed by the RLCG-MNA formulation [3] and the numerical integration is separately applied to the nodal and mesh equations. Here, the mesh equation rewritten with the reluctance matrix is solved for the current vector. Hideki Asai Shizuoka University hideasai@sys.eng.shizuoka.ac.jp

In the examples, we confirm the efficiency of the circuitbased FDTD method, comparing with SPICE simulators.

II. CIRCUIT BASED FDTD METHOD

A. RLCG-MNA Formulation

A mutually coupled system is compactly represented by the RLCG-MNA formulation [3]. The formulation can be understood for the example of the two conductor system shown in Fig. 1. The impedance of the coupled system is represented by two resistors, two self, and one mutual inductors. Then, the two nodes connecting resistor and inductor are not considered in the formulation. In the RLCG-MNA formulation, resistance matrix, the diagonal entries of which are a resistance value of conductors, appears in the (2,2) block part of the MNA matrix, though the part is a zero matrix in the original formulation.

The RLCG-MNA equation of the coupled system is written by

 $\mathcal{G} oldsymbol{x}(t) + \mathcal{C} rac{d}{dt} oldsymbol{x}(t) = oldsymbol{b},$

(1)

 $\boldsymbol{x}(t) = \begin{bmatrix} \boldsymbol{v}(t) \\ \boldsymbol{v}(t) \end{bmatrix}, \quad \boldsymbol{b} = \begin{bmatrix} \boldsymbol{J}(t) \\ \boldsymbol{J}(t) \end{bmatrix}$

where

$$\begin{aligned} \boldsymbol{x}(t) &= \begin{bmatrix} \boldsymbol{b}(t) \\ \boldsymbol{i}(t) \end{bmatrix}, \quad \boldsymbol{b} &= \begin{bmatrix} \boldsymbol{J}(t) \\ \boldsymbol{0} \end{bmatrix}, \\ \mathcal{G} &= \begin{bmatrix} \boldsymbol{G} & \boldsymbol{A}^T \\ -\boldsymbol{A} & \boldsymbol{R} \end{bmatrix}, \quad \mathcal{C} &= \begin{bmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{L} \end{bmatrix}. \end{aligned}$$

In (1), v(t), i(t), and J(t) are vectors of the node voltages, currents though inductors, and excited current sources, respectively. G, C, and A are conductance, capacitance, and incident matrices, respectively. The dimensions of these matrices and vectors in (1) are assumed as follows,

$$oldsymbol{v}(t) \in \mathcal{R}^n, oldsymbol{i}(t) \in \mathcal{R}^n, oldsymbol{J}(t) \in \mathcal{R}^n, \ oldsymbol{G}, oldsymbol{C} \in \mathcal{R}^{2n imes 2n}, oldsymbol{R}, oldsymbol{L} \in \mathcal{R}^{n imes n}, oldsymbol{A} \in \mathcal{R}^{n imes 2n}.$$

It is assumed here that in the equivalent RLC circuit of the mutually coupled system, each node is connected to the ground though a capacitor.

B. Circuit-based FDTD method

Yee's FDTD method [1] for solving the Maxwell's equations is based on the midpoint rule in the numerical integration and alternate updates of electric and magnetic fields. Shutt-Aine [2] provides a fast circuit simulation method for a large scale RLC network by replacing the electric and magnetic

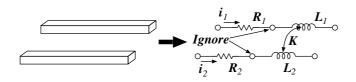


Fig. 1. Model of two conductor coupled system.

fields with the node voltages and branch currents in the circuit simulation. This method assumes that there exist a capacitor connected to the ground at every node and an inductor and resister branch between the two nodes. If the capacitor or inductor does not exist, a tiny capacitor or inductor, that is, latency is inserted. Therefore, this method is called Latency Insertion Method (LIM). Since a circuit does not always have such a capacitor and an inductor, we must often use latency which makes the simulation inaccurate. In [4], it is shown that necessity of inserting latency becomes mild by using the RLCG-MNA formulation (1).

Applying the midpoint rule to simulating (1), we can calculate the voltages and currents at a discrete time point as

$$\left\{\frac{1}{2}\boldsymbol{G} + \frac{1}{h}\boldsymbol{C}\right\}\boldsymbol{v}_{k+1} = -\left\{\frac{1}{2}\boldsymbol{G} - \frac{1}{h}\boldsymbol{C}\right\}\boldsymbol{v}_{k} \\ -\boldsymbol{A}^{T}\boldsymbol{i}_{k+1/2} + \boldsymbol{J}_{k+1/2}, \qquad (2) \\ \left\{\frac{1}{2}\boldsymbol{R} + \frac{1}{h}\boldsymbol{L}\right\}\boldsymbol{i}_{k+1/2} = -\left\{\frac{1}{2}\boldsymbol{R} - \frac{1}{h}\boldsymbol{L}\right\}\boldsymbol{i}_{k-1/2}$$

where $i_{k+1/2} = i(t_k + h/2)$, $v_k = v(t_k)$, and $h = t_{k+1} - t_k$. We call the procedure (2) and (3) the circuit-based FDTD method.

 $+Av_k$

III. METHOD USING RELUCTANCE MATRIX

In the RLCG-MNA equation (1), the conductance matrix G is always sparse and the capacitance C matrix is also sparse since the values are extracted by the window technique. Therefore, (2) is efficiently solved by using the sparse Cholesky decomposition. On the other hand, since it is not easy to discard the off-diagonal elements of inductance matrix with preserving the stability, the inductance matrix cannot be extracted partially. Therefore, solving (3) for the current vector needs a larger CPU cost than (2). Hence, the reluctance matrix K is introduced. The reluctance can be partially extracted [5], [6].

Multiplying $K = L^{-1}$ from the left side of (3), we can obtain the update rule for the current vector as

$$\left\{ \frac{1}{2} \boldsymbol{K} \boldsymbol{R} + \frac{1}{h} \boldsymbol{I} \right\} \boldsymbol{i}_{k+1/2} = - \left\{ \frac{1}{2} \boldsymbol{K} \boldsymbol{R} - \frac{1}{h} \boldsymbol{I} \right\} \boldsymbol{i}_{k-1/2} + \boldsymbol{K} \boldsymbol{A} \boldsymbol{v}_{k}.$$

$$(4)$$

The equation (4) is solved for the current vector by using the sparse LU decomposition. Fortunately, we can reduce the computational cost using the explicit numerical integration. In this case, solving the system of linear equations is not

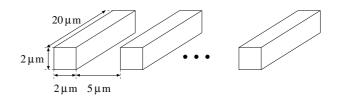


Fig. 2. Bus model.

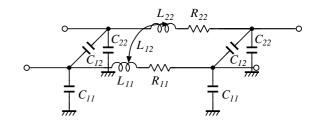


Fig. 3. Equivalent circuit of 2 bus model.

necessary. Using the forward Euler method, we can write the update rule as

$$i_{k+1/2} = (\boldsymbol{I} - h\boldsymbol{K}\boldsymbol{R}) i_{k-1/2} + h\boldsymbol{K}\boldsymbol{A}\boldsymbol{v}_k.$$
 (5)

Since the implicit numerical integration is used in (2), the timedomain simulation using (2) and (5) does not break down, if an appropriate time-step size is chosen [4].

IV. SIMULATIONS

To evaluate the circuit-based FDTD method, the bus model which consists of 128 conductors was analyzed, where these conductors were placed as shown in Fig. 2. Using FASTCAP [7], [8] and FASTHENRY [9], we calculated the capacitance and inductance matrices. Dividing the capacitance matrix into half, we made a equivalent circuit of the bus model. The case of the two conductors is shown in Fig. 3.

Terminating every node by a 50 $[\Omega]$ resister and giving an input current (0.1 [ns] fall/rise time, 0.4 [ns] pulse width, 0.2 [ns] delay time, 1.0 [ns] period, and 5 [mA] amplitude) at the node

 TABLE I

 CPU time Comparison of 128 conductors' Example

method	Implicit	Explicit
Full	0.64s	0.53s
SPARSE1	0.27s	0.20s
SPARSE2	0.18s	0.16s
HSPICE	12.36s	
NGSPICE	242.83s	

TABLE II CPU time Comparison of 2000 conductors' Example

method	Implicit	Explicit
Full	20.7s	10.9s
SPARSE1	4.81s	4.21s
SPARSE2	4.06s	3.80s

(3)

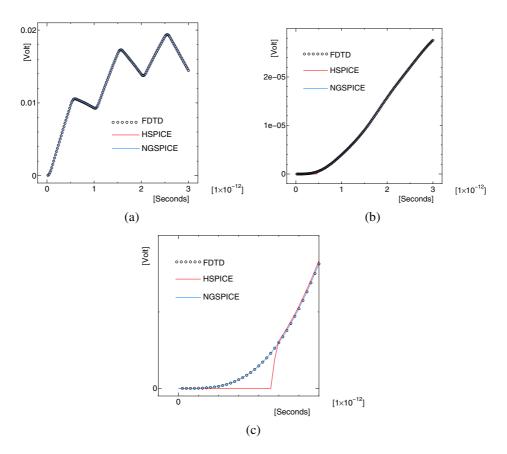


Fig. 4. Transient responses at (a)the nearest and (b)the farthest nodes from the input. (c)The enlarged responses of (b).

of the first conductor, we calculated the transient responses by the circuit-based FDTD method. For comparisons, the result is compared with HSPICE and Berkeley SPICE (NGSPICE). The transient responses at the nearest (input) and farthest nodes are shown in Figs. 4(a) and 4(b), respectively, where (4) is used for calculating the current vector. The CPU times are listed in Table 1, where the CPU time of the circuit-based FDTD method with the dense capacitance and inductance matrices is represented as 'Full', and 'implicit' and 'explicit' means that (4) and (5) are respectively used for calculating the currents. From Table 1, we can see that the proposed method is much faster than HSPICE and NGSPICE. The responses of Fig. 4(b) during (0, 0.7) [ps] are enlarged and shown in Fig. 4(c). The response of HSPICE is different from the others. Although HSPICE is faster than NGSPICE, it sacrifices the accuracy. Since the waveform obtained by the circuitbased FDTD method is identical to NGSPICE, this method is preferable to HSPICE and NGSPICE.

Fig. 5 shows the transient responses at the farthest node from the input, where the implicit integration of (4) or the explicit integration of (5) is used for calculating the current vector. Both responses are overlapped, which means that we can use the explicit numerical integration thought RLC circuits are usually stiff.

To evaluate the simulations with the sparse capacitance and inductance matrices, the capacitance and inductance matrices

were truncated so that they became a banded matrix. We made the banded inductance and capacitance matrices with bandwidths 21 and 11. The simulation results are shown in Figs. 6(a) and 6(b). We refer to the simulation using the banded matrices with bandwidth 21 as 'SPARSE1' and with bandwidth 11 as 'SPARSE2' in Figs. 6(a) and 6(b), and the case with the dense matrices as 'Full'. The transient waveforms of Figs. 6(a) and 6(b) show the responses at the far ends of the 10th and 20th conductors. Since the input is given at the first conductor, we can obtain a good approximation result if the observation node is within a distance corresponding to the bandwidth of the capacitance and inductance matrices. Therefore, in 'SPARSE2', we cannot expect a good approximation at the far end of 20th conductors as Fig. 6(b). We have to select an appropriate bandwidth in order to obtain a reasonable result. The CPU times of the simulations with the sparse matrices are also listed in Table 1.

As another example, the bus which has 2000 conductors with the same structure as the previous example, were analyzed. In this example, inductive coupling was only considered and a capacitor (0.126 [fF]) was connected to the ground at every node. We shows the CPU times of the simulations in Table 2 on the same conditions with 'SPARSE1', 'SPARSE2', and 'Full' of the previous example. Using the sparse matrices, the circuit-based FDTD method is certainly accelerated.

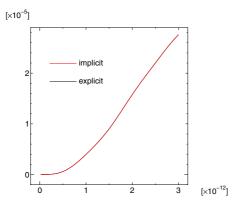


Fig. 5. Transient waveforms calculated by the circuit-based FDTD method, where the update rule (4) or (5) for current vector is used.

V. CONCLUSIONS

In this paper, the circuit-based FDTD method for analysis of a mutually coupled system has been presented, where the reluctance matrix is introduced. In this method, the voltage and current vectors are alternately updated. Therefore, this method is a variety of FDTD methods for circuit simulation. In the examples, the efficiency of the circuit-based FDTD method is shown, compared with SPICE simulators

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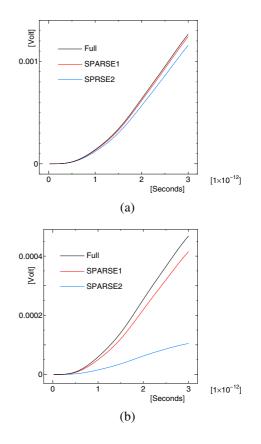


Fig. 6. Transient waveforms when the sparse capacitance and reluctance matrices are used. The responses at the far end of (a)the 10th and (b)the 20th conductors.