

# Measurement and Analysis of a CMOS Chaotic Spiking Oscillator Circuit That Acts as a Filter of Spike Trains

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## Abstract—

We have designed and fabricated a CMOS circuit that implements a chaotic spiking oscillator model, which acts as a filter of spike trains. This model is a phase oscillator that outputs a spike pulse at the timing of a predefined phase value, and transforms its phase value with a nonlinear transformation function at the timing of spike inputs. We have evaluated the fabricated circuit as a spike-train filter and show the measurement results for verifying the circuit operation. In addition, we show the difference between the measurement results of the fabricated circuit and the numerical simulation results of the model.

## 1. Introduction

Many oscillator models were proposed as a simple neuron model and a mathematical model expressing synchronization phenomena [1, 2, 3, 4]. The pulse-coupled oscillator model expresses information using pulse timing [4]. This model was implemented by discrete electronic circuits [5, 6, 7], CMOS integrated circuits [8] and FPGA circuits [9].

We have already proposed a chaotic spiking oscillator model that acts as a filter of spike trains [10]. This model can express various information by using the input-spike interval as a bifurcation parameter, and outputs various spike-train patterns including non-output states. In addition, this model can act as a low pass filter, a band stop filter and a filter combining both characteristics by varying the firing threshold.

We have designed and fabricated a CMOS circuit that implements this oscillator model using TSMC 0.25  $\mu\text{m}$  CMOS technology. In this paper, we show that evaluation results of the fabricated circuit.

## 2. Chaotic spiking oscillator model

This oscillator model is expressed by the following equations [10]:

$$x = \omega t \bmod x_{rst} \quad (1)$$

$$S_{out} = \begin{cases} 1 & \text{if } x = x_{th} \\ 0 & \text{if } x \neq x_{th} \end{cases} \quad (2)$$

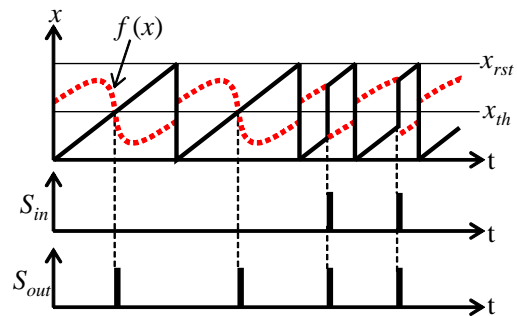


Figure 1: Timing diagrams of chaotic spiking oscillator model.

$$x \rightarrow f(x) \text{ if } S_{in} = 1 \quad (3)$$

where  $x$  is the internal state,  $\omega$  the natural frequency,  $t$  continuous time,  $x_{rst}$  the resetting threshold for the internal state,  $x_{th}$  the firing threshold, and  $f(\cdot)$  the nonlinear transformation function. Binary state  $S_{in}$  and  $S_{out}$  represent input and output spike timing, respectively.

Timing diagrams of this oscillator are shown in Fig. 1. We employed the chaotic neuron map [11] as  $f(\cdot)$ . Internal state  $x$  increases monotonically with  $\omega$ , outputs spike  $S_{out}$  when  $x$  exceeds  $x_{th}$  and is reset to zero when  $x$  reaches  $x_{rst}$ . When no spikes input, which means  $S_{in} = 0$ , this oscillator fires and outputs spike with constant period  $x_{rst}/\omega$ .

When spikes input ( $S_{in} = 1$ ), the oscillator converts  $x$  into  $f(x)$ . As a result, the inter-spike interval of  $S_{out}$  is changed nonlinearly, and depends on the timing of input-spikes. In addition, the oscillator cannot fire and output spikes when  $x$  continues to be mapped in a range of  $x < x_{th}$  or  $x > x_{th}$ .

## 3. CMOS circuit of chaotic spiking oscillator

Our oscillator circuit consists of a capacitor  $C_x$ , an oscillator circuit (OSC) part and a nonlinear voltage generator circuit (NVG) part, as shown in Fig. 2. The  $C_x$  holds the internal state voltage  $V_x$  at node  $P_x$ . The OSC charges or discharges  $C_x$ , and outputs spike  $S_{out}$  when the  $V_x$  exceeds

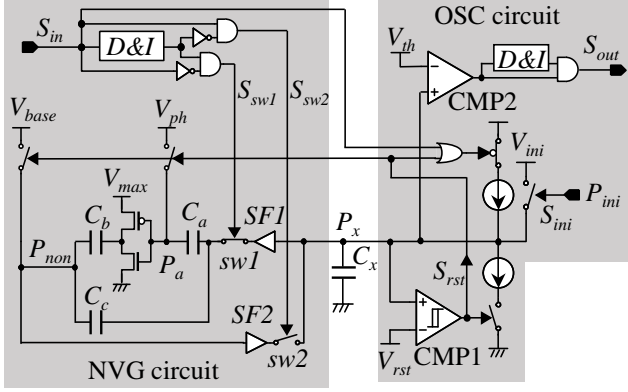


Figure 2: CMOS circuit of chaotic spiking oscillator.

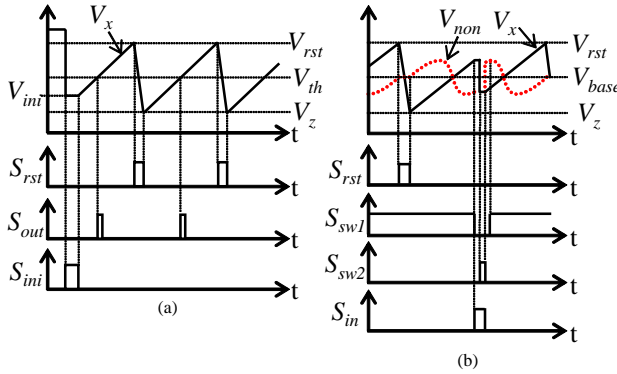


Figure 3: Timing diagrams of chaotic spiking oscillator circuit: (a) OSC part and (b) NVG part.

$V_{th}$ . The NVG converts the  $V_x$  into nonlinear voltage  $V_{non}$  at node  $P_{non}$  when spikes input:  $S_{in} = 1$ . Timing diagrams of the circuit are shown in Fig. 3.

### 3.1. Operation of OSC circuit

The OSC circuit consists of two switched-current sources that charge or discharge  $C_x$ , a hysteresis comparator (CMP1) that compares  $V_x$  with resetting threshold voltage  $V_{rst}$  and outputs reset signal  $S_{rst}$ , a comparator (CMP2) that compares  $V_x$  with threshold voltage  $V_{th}$  and a delay-and-inversion circuit (D&I) and an AND gate that generates  $S_{out}$ . The circuit operation is as follows:

- 1) Voltage  $V_x$  is initialized at  $V_{ini} (< V_{rst})$  by initialization signal  $S_{ini}$ , and the OSC begins to oscillate.
- 2) Capacitor  $C_x$  is charged by the current source and  $V_x$  increases with a constant speed.
- 3) When  $V_x$  exceeds  $V_{th}$ , the CMP2 output turns over, and output spike signal  $S_{out}$  is generated by a D&I and an AND gate.
- 4) When  $V_x$  reaches  $V_{rst}$ , the CMP1 outputs  $S_{rst} = 1$  and  $V_x$  is reset to voltage  $V_z$  by the constant current source.
- 5) Repeat 2) to 4) when  $S_{in} = 0$ .

Table 1: Specification of a fabricated circuit

Technology	TSMC 0.25 $\mu\text{m}$ CMOS
Layout area	137.43 $\times$ 155.4 $\mu\text{m}^2$
Power supply voltage	3.3 V
Operating frequency ( $\omega$ )	0.2 Hz-713 kHz
Power consumption	589 $\mu\text{W}$ (at $\omega = 167$ kHz)

Here, the time span of  $S_{rst} = 1$  is determined by the hysteresis characteristic of CMP1, and  $V_z$  is determined by the time and the current for discharging  $C_x$  from  $V_{rst}$ .

### 3.2. Operation of NVG circuit

The NVG circuit consists of two source-follower analog buffers SF1 and SF2, three capacitors  $C_a$ ,  $C_b$  and  $C_c$ , a CMOS inverter, two switches sw1 and sw2, a delay-and-inversion circuit (D&I), two AND gates and two NOT gates. This circuit generates nonlinear voltage  $V_{non}$  at node  $P_{non}$  by adding  $V_x$  to the CMOS inverter output voltage that is generated from  $V_a$  at node  $P_a$ . Nonlinear voltage  $V_{non}$  and  $V_a$  are set to  $V_{base}$  and  $V_{ph}$  by reset signal  $S_{rst}$ , respectively. As a result, the voltage and phase of  $V_{non}$  are shifted by  $V_{base}$  and  $V_{ph}$ , respectively.

The sw1 and the sw2 are switched by signals  $S_{sw1}$  and  $S_{sw2}$  that are generated from  $S_{in}$  as follows:

- 1) Switch sw1 is turned off by  $S_{sw1} = 0$ . Then,  $C_b$  and  $C_c$  generate  $V_{non}$  that is determined by  $V_x$  at the timing when  $S_{in}$  becomes "High".
- 2) After sw2 is turned on by  $S_{sw2} = 1$ , the voltage held at  $C_x$  at node  $P_x$  is varied from  $V_x$  to  $V_{non}$ .
- 3) Switch sw2 is turned off by  $S_{sw2} = 0$ .
- 4) Switch sw1 is turned on by  $S_{sw1} = 1$ .

Here, the intervals 1)-2) and 3)-4) are determined by the D&I circuit.

Consequently,  $V_{non}$  is given by the following equation:

$$V_{non}(t) = \frac{C_b u(V_x(t) - V_z + V_{ph}) + C_c V_x(t)}{C_b + C_c} + V_{base} - \frac{C_b u(V_{ph}) + C_c V_z}{C_b + C_c} \quad (4)$$

where  $u(\cdot)$  is the input-output characteristic of the CMOS inverter. Note that the maximum value of  $u(\cdot)$  is determined by the supply voltage  $V_{max}$  of the CMOS inverter.

### 4. Measurement and analysis

We designed and fabricated the CMOS circuit using TSMC 0.25  $\mu\text{m}$  CMOS technology, where we set  $C_b = 289$  fF and  $C_c = 900$  fF. The specification of the fabricated circuit is shown in Table 1.

We investigated the relationship between inter-spike intervals of  $S_{out}$ ,  $T_{out}$ , and a fixed inter-spike interval of  $S_{in}$ ,

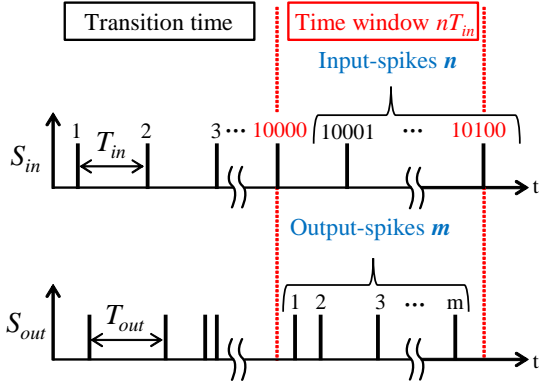


Figure 4: Measurement condition for input and output spikes.

$T_{in}$ , and that of the firing rate  $m/n$  and  $T_{in}$ , where  $n$  and  $m$  are the numbers of input and output spikes during the time span of the measurement period, respectively. Namely, the time-window for measurement is  $nT_{in}$ , as shown in Fig. 4. The measurements were performed after giving 10,000 input-spikes that is assumed to be transition time. We set here  $n = 100$ ,  $V_{max} = 3.3$  V,  $V_{ph} = 0.96$  V,  $V_{base} = 1.70$  V,  $V_{rst} = 2.2$  V and  $(V_{rst} - V_z) = 1.0$  V.

Measurement results about  $T_{out}$  and  $m/n$  are shown in Fig. 5, when we change  $T_{in}$  from 268 ns to 7000 ns at a step of 4ns. We set here  $V_{th} = 1.635$  V. From Fig. 5, we can observe some chaotic behaviors in the bifurcation phenomena.

Measurement results about  $m/n$  are shown in Fig. 6, when  $T_{in}$  and  $V_{th}$  are changed from 268 ns to 6988 ns at a step of 40ns and from 1.185 V to 2.135 V at a step of 0.025 V, respectively. We see from Fig. 6 that the oscillator acts as the following filters: a low-pass filter at  $V_{th} = 1.260$  V, a band-stop filter at  $V_{th} = 1.860$  V and a filter combining both characteristics at  $V_{th} = 1.410$  V.

We found from Fig. 5(a) that the measurement results are different from those of numerical results around  $T_{in} = 4000$ ns. The reason of this difference is discussed below.

The proposed model [10] assumes that fall time  $T_f$  is negligibly small, as shown in Fig. 7(a). However, the fabricated circuit has a finite  $T_f$ , as shown in Fig. 7(b). We investigated an influence of the fall time at  $V_{th} = 1.635$  V and  $T_{in} = 3700$  ns. Figure 8 shows time-series of  $V_x$ ,  $V_{non}$ ,  $S_{in}$  and  $S_{out}$  observed in an oscilloscope, where some of the input spikes  $S_{in}$  were fed into the circuit during the falling periods of  $V_x$ .

We also investigated the influence by comparing the case of  $T_f = 0$  with that of  $T_f = T_n/13$  by numerical simulation, where  $T_n$  is the natural period, that is the inverse of  $\omega$ . Nonlinear function  $f(\cdot)$  is based on the chaotic neuron map, as described in Sec. 2:

$$f(x) = 0.54x + 0.57/[1 + \exp\{(x - 0.5) * 60\}] - 0.11 \quad (5)$$

where  $x$  is in the range of  $0 \leq x \leq 1$ . We set here  $x_{th} = 0.47$ .

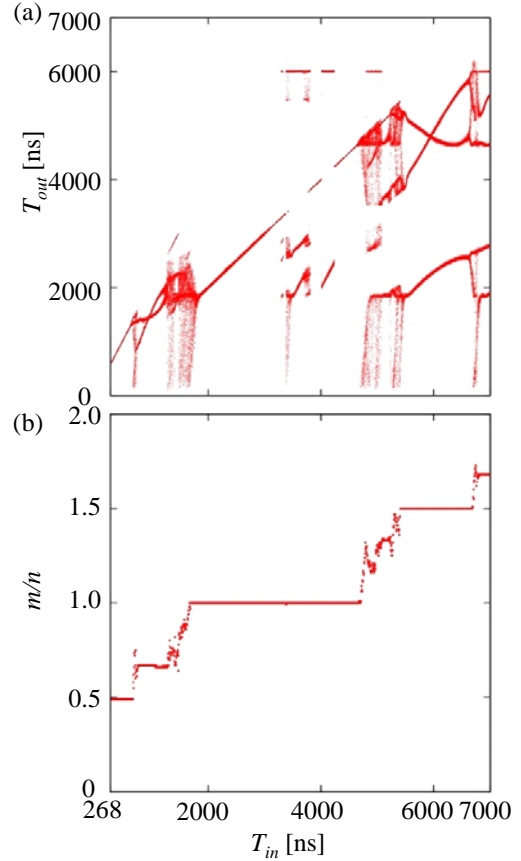


Figure 5: Output-spike interval  $T_{out}$  and firing rate  $m/n$  as a function of  $T_{in}$ , where we set  $V_{th} = 1.635$  V.

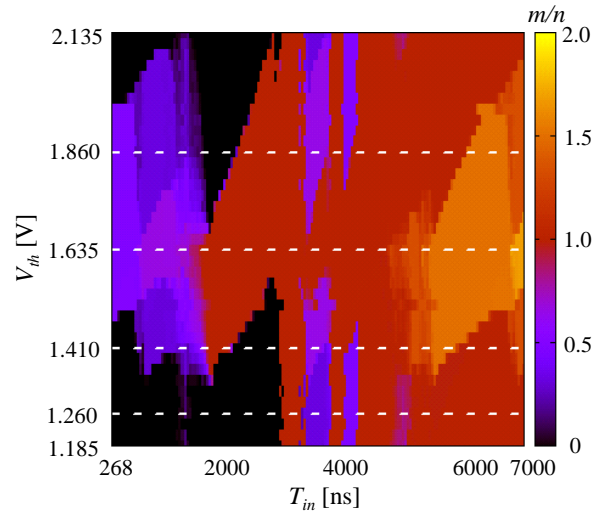


Figure 6: Firing rate  $m/n$  when  $T_{in}$  and  $V_{th}$  are changed.

The numerical simulation results are shown in Fig. 9. We can see the difference between the two, and the result with finite  $T_f$  (Fig. 9(b)) is more similar to the measurement result (Fig. 5(a)) than the ideal result (Fig. 9(a)).

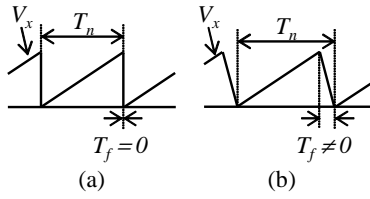


Figure 7: Definition of fall time  $T_f$  and natural period  $T_n$ : (a) ideal model and (b) model including the fall time.

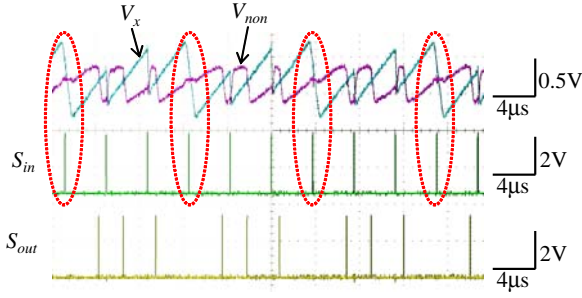


Figure 8: Time-series of  $V_x$ ,  $V_{non}$ ,  $S_{in}$  and  $S_{out}$  observed in an oscilloscope, where  $T_{in} = 3700$  ns.

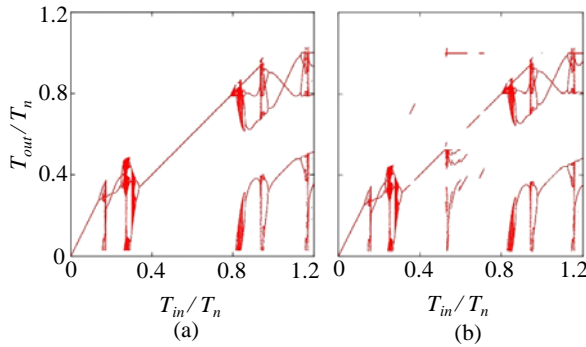


Figure 9: Numerical simulation Results about the relationship between  $T_{in}/T_n$  and  $T_{out}/T_n$ , where  $x_{th} = 0.47$ : (a)  $T_f = 0$  and (b)  $T_f = T_n/13$ .

## 5. Conclusions

We evaluated the fabricated CMOS circuit of a chaotic spiking oscillator as a spike-train filter and showed the measurement results for verifying the circuit operation. We showed that the fabricated circuit exhibits bifurcation phenomena by varying input-spike interval and acts as a low pass filter, a band stop filter, and a filter combining both characteristics by varying the firing threshold. In addition, we confirmed that the fall time influences the bifurcation characteristics by showing results of the numerical simulation. In future work, we will construct an oscillator network consisting of the fabricated CMOS circuits, and will conduct experiments about network operation.

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