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# An Implementation Technique of a $\beta$-A/D Converter with a Unity-Gain Buffer

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**Abstract**—We propose an implementation technique of a $\beta$-A/D converter circuit with unity-gain buffer (UGB). In the circuits based on UGBs, the gain error of the UGB is critical. We confirm the functionality and robustness of the proposed circuit against the variations in the gain of the UGB through SPICE simulations using ideal elements.

## 1. Introduction

Thanks to advanced semiconductor microfabrication processes, the performance of digital integrated circuits has improved. However, it is difficult to realize high-performance analog integrated circuits owing to the low transconductance $g_m$ of advanced microfabrication transistors and the mismatches between the circuit elements. The importance of analog-to-digital (A/D) converters has been increasing in current digital era. Therefore, a circuit technique that implements a high-performance A/D converter is indispensable.

A $\beta$-encoder ($\beta$-A/D converter circuit) using a real number conversion radix $\beta$ ($1 < \beta < 2$) [1–3] is an A/D converter circuit that is robust against the fluctuations in the offset and threshold voltages of a comparator circuit. In addition, we can estimate the real value of $\beta$ realized in the actual circuit from the output bit sequences using a characteristic equation with exponential accuracy. Therefore, we do not need to realize the values of $\beta$ very accurately. That is, a high-gain opamp is not required to accurately realize the value of $\beta$. Consequently, the $\beta$-A/D converter circuits are robust against the fluctuations and mismatches in the constituent device characteristics; therefore, they are suitable for a high-performance IC implementation through advanced semiconductor microfabrication processes.

IC implementation techniques for $\beta$-A/D converter circuits have already been proposed with IC prototyping [4–9]. In these studies, a method that estimates the realized $\beta$ value by the circuit suitable for the ICs, the theoretical formulas of the conversion errors, and the $\beta$ to binary conversion circuits were proposed. The high performance and robustness of the IC implementations of the cyclic and pipeline $\beta$-A/D converter circuits, which were designed on the basis of the proposed design procedure, have been demonstrated.

The above $\beta$-A/D converter circuits adopted and expanded the basic configuration of ordinary binary A/D converters. Moreover, a unity-gain buffer (UGB) has been used to improve the conversion speed for an ordinary binary A/D converter [10]. Therefore, we proposed a circuit implementation technique of the $\beta$-A/D converter circuit with the UGB [11]. However, in [11], we only showed the conceptual circuit. In particular, an additional sample-and-hold (S/H) circuit was used to clearly show the circuit operations. In this paper, we propose a practical circuit implementation technique of the $\beta$-A/D converter circuit with the UGB. In circuits based on UGBs, the gain error of the UGB is critical. Therefore, we investigate the effects of the UGB gain error on the conversion characteristics of the proposed $\beta$-A/D converter circuits through SPICE using ideal circuit elements. In addition, the effects of the parasitic capacitances are also considered and simulated through SPICE. As a result, we confirm that both the gain error and parasitic capacitances do not deteriorate the conversion characteristics if we use the value of $\beta$ estimated from the output bit sequences.

## 2. A/D Converter based on the $\beta$-map

A $\beta$-transformation, which is the basis of the $\beta$-A/D converter circuit, is given as [1–3],

$$x(t_{n+1}) = \begin{cases} \beta x(t_n), & x(t_n) \in [0, \theta) \\ \beta x(t_n) - (\beta - 1), & x(t_n) \in [\theta, (\beta-1)^{-1}), \end{cases} \quad (1)$$

where $x(t_n) \in [0, (\beta-1)^{-1}]$ is the internal state of the converter, $1 < \beta < 2$ is the conversion radix, $t_n$ is the discrete time ($n = 1, 2, \ldots$), and $\theta$ is the threshold. The quantizer $Q_\theta(t_n)$, which gives the resulting bit sequence $b(t_n) \in \{0, 1\}$, is defined as

$$b(t_n) = Q_\theta(x(t_n)) = \begin{cases} 0, & x(t_n) < \theta \\ 1, & x(t_n) \geq \theta. \end{cases} \quad (2)$$

By using Eq. (2), we can rewrite Eq. (1) as

$$x(t_{n+1}) = \beta x(t_n) - (\beta - 1) \cdot b(t_n). \quad (3)$$

The $\beta$-A/D converter circuit would function properly, even the value of $\theta$ varies, if $\beta^{-1} \leq \theta \leq \beta^{-1}(\beta-1)^{-1}$. Using the $\beta$-A/D converter with the full-scale of $V_{FS}$ and the conversion bit-length $L$, the input voltage $V_{input}$ is $\beta$-expanded as

$$\frac{V_{input}}{V_{FS}} \fallingdotseq (\beta - 1) \sum_{i=1}^{L} b(t_i) \cdot \beta^{-i}. \quad (4)$$

## 3. $\beta$-A/D converter with the UGB

The conceptual schematics for the $\beta$-A/D converter circuits using the UGB were proposed in [11], where an auxiliary S/H circuit was introduced to explain the circuit operations. In Fig. 1, a practical circuit of the $\beta$-A/D converter with the UGB is proposed on the basis of the circuit in [11]. In Fig. 1, the function of the S/H circuit is implicitly included in the circuitry. Figure 2 shows the clock waveforms that drive the proposed circuit. In the following, we briefly explain the operation of the proposed circuit in Fig. 1.

First, in the waveforms in Fig. 2, when $t = t_{\frac{1}{2}}$, the input voltage $V_{input}(t_{\frac{1}{2}})$ is sampled to $C_h$ by $\phi$S.

Next, $\phi$1 is high at $t = t_1$; then, $V_i(t_1) = V_{input}(t_{\frac{1}{2}})$. This voltage is transfered through the UGB, resulting in $V_o(t_1) = V_i(t_1)$. At the same time, the voltage $V_o(t_1)$ is compared to the threshold voltage $V_\theta$ by the comparator. The output of the comparator $b(t_1)$, which will be the most significant bit (MSB) of the conversion bit sequence, is 0 if $V_o(t_1) < \theta$; otherwise, it is 1. Here, $b(t_1)$ controls the multiplexer (MUX) $V_M$ in such a way that $V_M = V_{ref}$ when $b(t_1) = 1$, and $V_M = 0$ when $b(t_1) = 0$.

At $t = t_{1+\frac{1}{2}}$, $\phi$2 is high, and the charge on $C_f$ is transfered to $C_s$ and $C_h$. As a result, the output voltage of the UGB $V_o(t_{1+\frac{1}{2}})$ becomes

$$V_o(t_{1+\frac{1}{2}}) = \frac{C_s + C_h + C_f}{C_s + C_h} \cdot V_i(t_1) - \frac{C_f}{C_s + C_h} \cdot V_{ref} \cdot b(t_1). \quad (5)$$

Comparing Eq. (3) and Eq. (5), we can realize the $\beta$-A/D converter function if we set the capacitances as

$$C_s + C_h : C_f \quad = \quad 1 : \beta - 1. \quad (6)$$

Finally, at $t = t_2$ when $\phi$1 is high, $V_i(t_2)$ is sampled on $C_s$, and $V_o(t_2) = V_i(t_2)$. Consequently, we can write

$$V_o(t_2) = \beta V_i(t_1) - (\beta - 1) \cdot V_{ref} \cdot b(t_1). \quad (7)$$

This concludes one iteration. Repeating the same procedure until $t = t_L$, we finally obtain

$$V_o(t_{n+1}) = \beta V_i(t_n) - (\beta - 1) \cdot V_{ref} \cdot b(t_n), \quad (8)$$

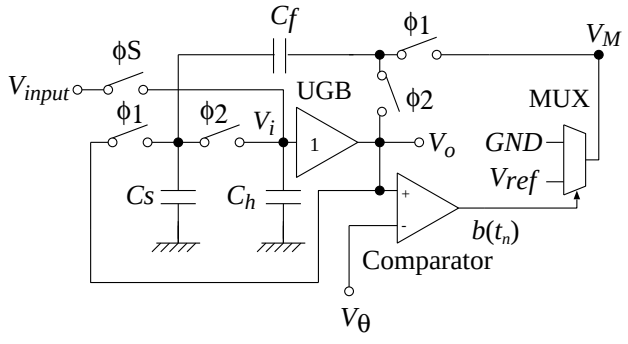


Figure 1: The $\beta$-A/D converter circuit with the UGB.

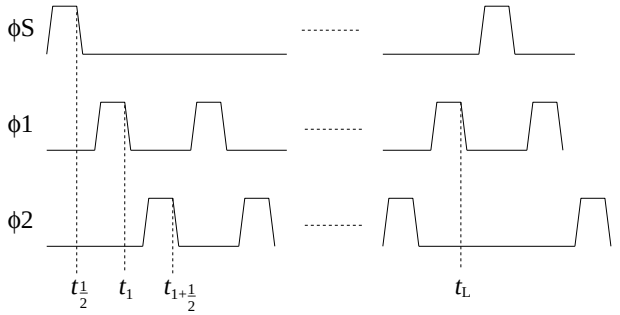


Figure 2: The clock waveforms for the circuit in Fig. 1.

where $1 \le n \le L - 1$. This confirms that the proposed circuit shown in Fig. 1 realizes the $\beta$-A/D converter circuit.

## 4. Fully differential $\beta$-A/D converter circuit

The circuit proposed in Fig. 1 is single-ended. The fully differential configuration is mandatory for practical A/D converter circuits. Figure 3 shows the fully differential version of the $\beta$-A/D converter circuit in Fig. 1. The clock waveforms for the circuit in Fig. 3 are the same as those in Fig. 2. In Fig. 3, the parasitic capacitances, $C_{p1}, C_{p2}$, and $C_{p3}$, are also included. The voltage $V_o(t_{n+1}) \equiv V_o^+(t_{n+1}) - V_o^-(t_{n+1})$ is given by

$$\begin{aligned} V_o(t_{n+1}) &= \frac{C_f + C_s + C_h + C_{p1} + C_{p2} + C_{p3}}{C_s + C_h + C_{p1} + C_{p2} + C_{p3}} \cdot V_i(t_n) \\ &- \frac{C_f}{C_s + C_h + C_{p1} + C_{p2} + C_{p3}} \cdot V_{ref} \cdot b(t_n) \\ &= \frac{C_f + C_s + C_h + X}{C_s + C_h + X} \cdot V_i(t_n) \\ &- \frac{C_f}{C_s + C_h + X} \cdot V_{ref} \cdot b(t_n), \end{aligned} \quad (9)$$

where $V_i(t_n) \equiv V_i^+(t_n) - V_i^-(t_n)$, and $X = C_{p1} + C_{p2} + C_{p3}$. If we define

$$\beta = \frac{C_f + C_s + C_h + C_X}{C_s + C_h + C_X}, \quad (10)$$

Eq. (9) can be reduced to Eq. (8). This confirms that the circuit in Fig. 3 realizes the $\beta$-A/D converter and is parasitic insensitive. In addition, the value of $\beta$ in Eq. (10) can be obtained with arbitrary precision from the bit-sequences with the $\beta$-estimation technique proposed in [4].

### 4.1. SPICE simulations

We simulated the proposed circuit in Fig. 3 through SPICE using ideal circuit components in order to show the effects of the parasitic capacitances and the UGB gain errors on the conversion characteristics. Table 1 summarizes the capacitances used in the simulations. In addition, we changed the gain of the UGB, $A_{UGB}$, from 0.8 to 1 in increments of 0.05.

First, Fig. 4 shows the estimated value of $\beta$, $\beta_{eff}$, when we changed $A_{UGB}$, for different values of the designed

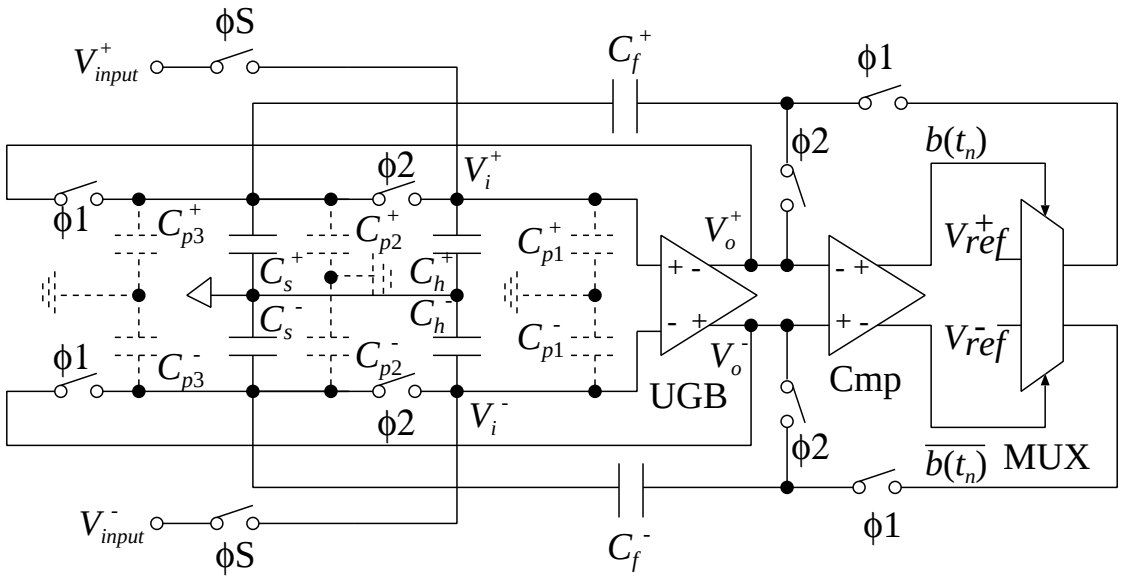


Figure 3: The fully differential $\beta$-A/D converter circuit with the UGB.

$\beta_d$ ($\beta_d$ =1.8 and 1.9), which is given by Eq. (9) with $X = 0$ and $A_{UGB} = 1$. Table 2 shows the bit-length $M$ used for $\beta$-estimations. From Fig. 4, it can be seen that $\beta_{eff} \neq \beta_d$ because of the nonunity gain of the UGB and the parasitic capacitances.

Second, Fig. 5 shows the conversion characteristic for different values of $A_{UGB}$. To decode the resulting bit sequences, we used the values of $\beta_{eff}$ in Fig. 4. In addition, the bit-length $L$ was determined according to Eq. (11) to obtain an effective resolution of 10-bits in the binary expansions [5].

$$L > \frac{N+1}{\log_2 \beta_{eff}} \tag{11}$$

As shown in Fig. 5, the conversion gain decreases as $A_{UGB}$ decreases. However, the linearity, which is one of the most important characteristics of A/D converters, is intact, even with low $A_{UGB}$ and parasitic capacitors.

The third simlation in Fig. 6 shows the effective number of bits (ENOB) for different values of $A_{UGB}$. In the simulations, the bit-length $L$ was determined by Eq. (11) to obtain an effective binary resolution of 10 bits. The ENOB was calculated from the spectrum with a sinusoidal input, as shown in Fig. 6. The results in the figure confirm that

Table 1: Capacitances used in the simulations.

| Capacitance | Value [fF] |
|---|---|
| $C_s$ | 140 |
| $C_h$ | 140 |
| $C_f$ | 224, 252 |
| X | 5 |

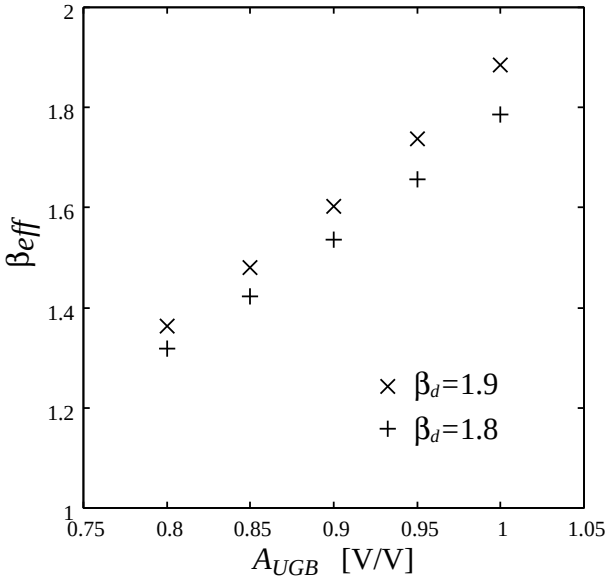


Figure 4: The estimated value of $\beta$, $\beta_{eff}$, when we change $A_{UGB}$ for the designed values of $\beta_d$ =1.8 and 1.9.

Table 2: Bit-length $M$ for $\beta$-estimation.

| $A_{UGB}$ [V/V] | $\beta_d$ (Designed $\beta$) | |
|---|---|---|
| | $\beta_d$ = 1.8 | $\beta_d$ = 1.9 |
| 1 | 20 | 20 |
| 0.95 | 20 | 20 |
| 0.9 | 20 | 20 |
| 0.85 | 40 | 30 |
| 0.8 | 50 | 40 |

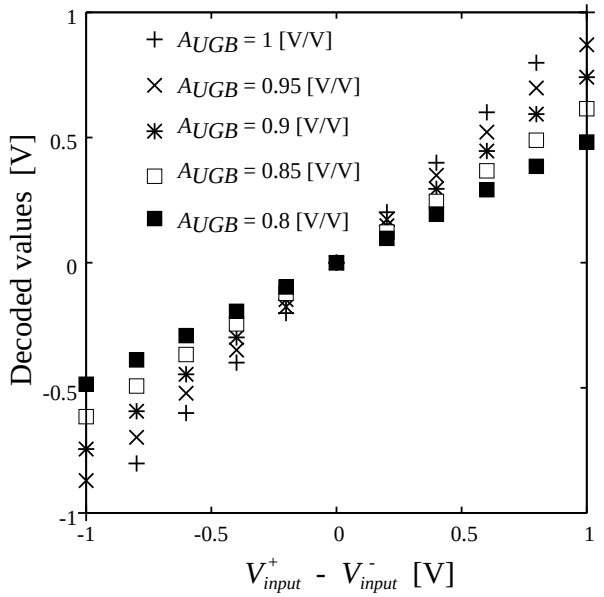


Figure 5: The conversion characteristics of the proposed $\beta$-A/D converter circuit with different values of $A_{UGB}$

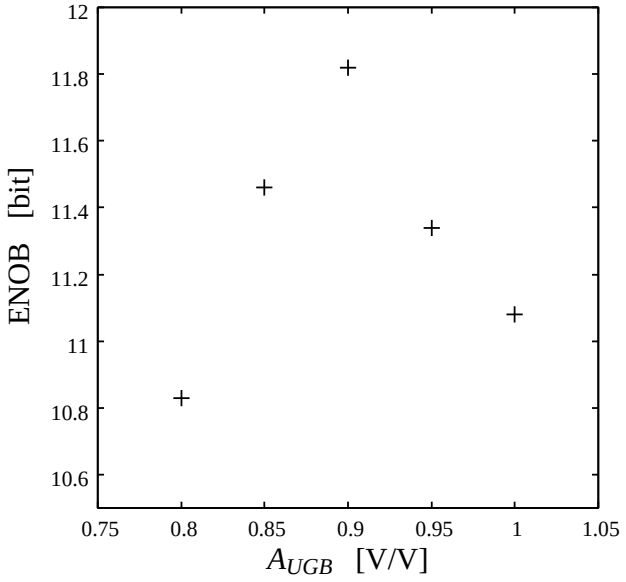


Figure 6: The effective number of bits when we change the value of $A_{UGB}$

we can obtain values for the ENOB that are greater than 10 bits, even with $A_{UGB} < 1$ and parasitic capacitors.

## 5. Conclusion

We have proposed practical circuits of a $\beta$-A/D converter with a UGB on the basis of the conceptual circuits in [11]. The effects of the errors on the UGB gain (nonunity gain) and parasitic capacitances have been investigated through SPICE simulations. As a result, we have confirmed that the proposed circuit is robust against the gain error and parasitic capacitors. In our future work, we will implement the proposed circuit as an integrated circuit and experimentally confirm the advantage of the UGB configuration employed in the proposed citcuit.


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