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Simplified Architecture for Cellular Neural Network suitable for High-Density Integration of Electron Devices

Mutsumi Kimura[†,‡], Ryohei Morita[†], Yuki Koga[†], Hiroki Nakanishi[†], Nao Nakamura[†], and Tokiyoshi Matsuda[†]

†Department of Electronics and Informatics, Ryukoku University
Seta, Otsu 520-2194, Japan
‡Graduate School of Information Science, Nara Institute of Science and Technology
Takayama, Ikoma 630-0192, Japan
Email: mutsu@rins.ryukoku.ac.jp

Abstract– We will propose a simplified architecture for a cellular neural network suitable for high-density integration of electron devices. A neuron consists of only eight transistors, and a synapse consists of just only one variable resistor. First, we developed a specialized simulator to estimate the practical operation. Moreover, we emulated the neural network using a field-programmable gate array and trimming resistors. The neural network succeeded in learning multiple logics even in a small-scale network. We think that this result indicates that our proposal has a big potential for future electronics using neural networks.

1. Introduction

Cellular neural networks are neural networks where a neuron is connected to only neighboring neurons [1], hence suitable for integration of electron devices, and promising for image processing [2], pattern recognition [3], etc. Until now, fundamental theory, working principle, and application potential have been actively investigated using formal models and numerical simulation. However, there exist few reports on actual hardware of cellular neural networks [4], although they are suitable for integration of electron devices as aforementioned. We imagine that this is because the conventional circuits of the neurons and synapses are still complicated, even though the structure of the network is simple.

We are developing neural networks from the viewpoint of device hardware [5],[6]. In this presentation, we will propose a simplified architecture for a cellular neural network suitable for high-density integration of electron devices. The main advantage is that the circuits of the neurons and synapses are excellently simplified. A neuron consists of only eight transistors, and a synapse consists of just only one variable resistor. As a result, the neural network must have a different structure and modified procedure for the recalling and learning from the conventional one, and hence we would like to evaluate them before actual integration of electron devices. First, we developed a specialized simulator to estimate the practical operation. Moreover, we emulated the neural network using a field-programmable gate array (FPGA) and trimming resistors. The neural network succeeded in learning multiple logics, such as AND, OR, and XOR, even in a small-scale network, such as 3 × 3. Although this result is primitive, we think that it indicates that our proposal has a big potential for future electronics using neural networks.

2. Simplified Architecture

2.1. Neuron

Figure 1 shows the neuron. We limited the necessary functions of the neuron to that a binary state is maintained by itself and altered by the input signals. In order to realize this simple function, we adopted a latch circuit that circularly connects two inverters with two switches. The firing or non-firing state is maintained using the latch circuit when the switches are turned on, namely, we defined the firing state as a situation when the voltages at node α and node β are high and complementarily low, respectively, whereas we defined the non-firing state as the opposite situation. Although the latch circuit is a well-known circuit for maintaining a binary state, it should be noted that its characteristic is similar to a sigmoid function, a typical function used to provide a favorable soft threshold in neural network models. The binary state is altered after the switches are turned off, the input signals are applied to nodes α and β, and the switches are turned on again. In any case, by employing complementary inverters and switches, we succeeded in making a neuron consist of only eight

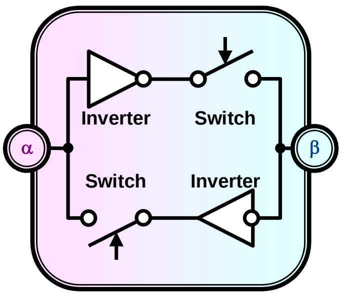

Fig. 1. Neuron.

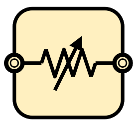

Fig. 2. Synapse.

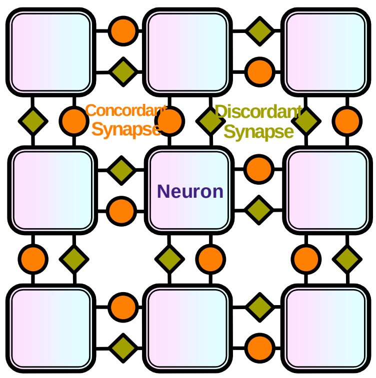

Fig. 3. Neural network.

transistors.

2.2. Synapse

Figure 2 shows the synapse. We limited the necessary functions of the synapse to that an input signal from a neuron is weighted by its synaptic connection strength and transferred to another neuron, and the synaptic connection strength is adjusted. In order to realize this simple function, we adopted a variable resistor. An input voltage from a neuron is weighted by the conductance of the variable resistor and transferred to another neuron. The synaptic connection strength corresponds to the conductance of the variable resistor, which is adjusted obeying a modified Hebbian learning as belowmentioned. In any case, we succeeded in making a synapse consist of just only one resistor.

2.3. Neural network

Figure 3 shows the neural network. Because the neuron and synapse are dramatically simplified, although the neural network is still classified into a kind of cellular neural networks, it must have a different structure from the conventional one. We arrayed the neurons and connected each neuron to only up, down, left, and right neighboring neurons through the synapses. In order to compensate the small number of the synapses, we connected neurons through a pair of synapses, namely, concordant and discordant synapses. The concordant synapse is connected between the same nodes in the two neurons, nodes α and α or β and β, and inclines to make the states of the two neurons the same, whereas the discordant synapse is connected between different nodes, nodes α and β, and inclines to make the states of the two neurons different. All the input voltages from all the neighboring neurons are weighted by the conductances of all the concordant and discordant synapses and transferred to the target neuron. The target neuron becomes the firing or non-firing state. As a result, the binary state of the target neuron is determined by the majority rule of the binary states of the neighboring neurons with weighted by the synaptic connection strengths. Moreover, it should be noted that this network is also classified into a kind of interconnective neural networks, where a synapse transfer a signal from a neuron to another neuron and simultaneously from the latter neuron to the former neuron vice-versa, namely, the synapses are bidirectional, which may correspond to functions of two synapses and also compensate the small number of the synapses. In any case, we succeeded in making a cellular neural network, where we connected each neuron to only neighboring neurons, which is exceedingly suitable for high-density integration of electron devices.

3. Modified Hebbian learning

Figure 4 shows the modified Hebbian learning. Because the neuron and synapse are dramatically simplified, the neural network must also have a modified procedure for the learning from the conventional one. Hebbian learning is a typical learning procedure in biological and artificial neural networks [7]. The synaptic connection strength is enhanced when both neurons connected to the synapse are in firing states and impaired otherwise. Based on the Hebbian learning, we will propose the modified Hebbian learning as shown in Fig. 4. Here, we assume NOT logic as an example. The left and right neurons are assigned to input and output elements, respectively. Initially, at the initial recalling stage, a non-firing state is applied to the input element, and a non-firing state arises from the output elements, and vice versa because the synaptic connection strength of the concordant synapse is accidentally slightly stronger than that of the discordant synapse, which is not NOT logic. Next, at the first learning stage, a non-firing state is applied to the input element, and a firing state is applied to the output element. Since the concordant synapse is connected between the same nodes in the two neurons, and the binary states at both nodes in two neurons are different, electric current flows through the concordant synapse because of the voltage difference, whereas electric current does not flow through the discordant synapse. Consequently, the characteristic degradation gradually occurs at the concordant synapse, which is a necessary property of our synapses, the conductivity becomes gradually lower, and the synaptic connection strength becomes gradually weakened, whereas the characteristic enhancement gradually occurs at the discordant synapse, which is another necessary property of our synapses, the conductivity becomes gradually higher, and the synaptic connection strength becomes gradually strengthened. At the second learning stage, a firing state is applied to the input element, and a non-firing state is

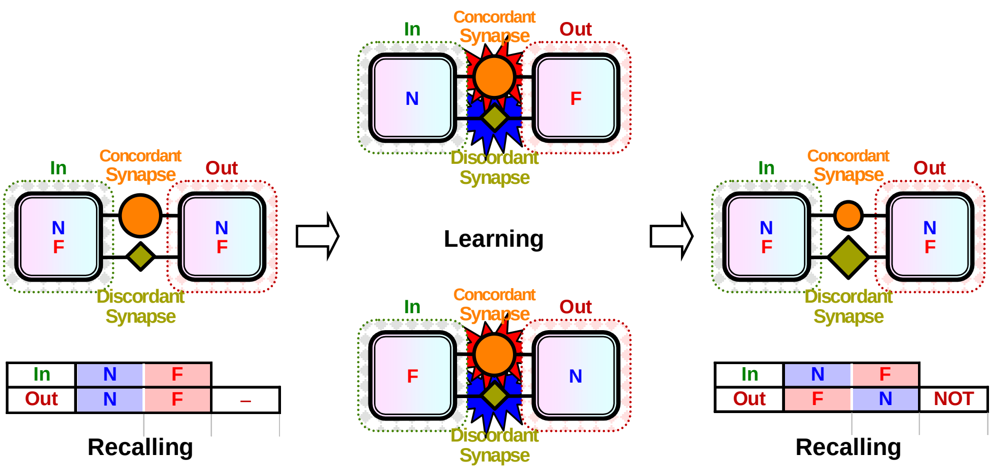

Fig. 4. Modified Hebbian Learning.

applied to the output element. Similarly, the synaptic connection strength of the concordant synapse becomes gradually weakened, whereas the synaptic connection strength of the discordant synapse becomes gradually strengthened. Finally, at the final recalling stage, a non-firing state is applied to the input element, and a firing state arises from the output elements, and vice versa because the synaptic connection strength of the discordant synapse becomes slightly stronger than that of the concordant synapse, which is NOT logic. It should be noted that these necessary properties of our synapses can be obtained using memristors [8], which is also suitable for high-density integration of electron devices. Because the synaptic connection strengths become both weakened and strengthened, we call this procedure modified Hebbian learning. In any case, by employing the modified Hebbian learning, we succeeded in making a synapse consist of just only one resistor.

4. Specialized simulator

Figure 5 shows the formal model. The neuron receives input signals and sends output signals, and each neighboring neuron from which the input signal is received is the same as that to which the output signal is sent, which means that the synapses are bidirectional. The operation of this formal model can be approximately described using the following difference equation:

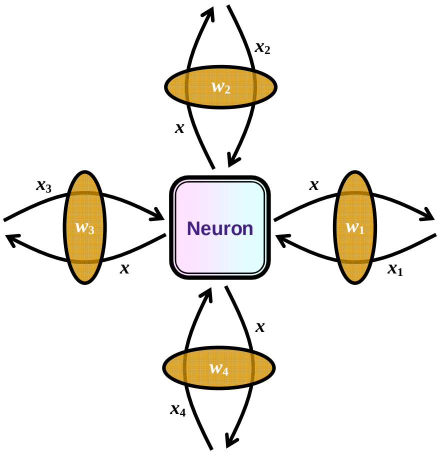

Fig. 5. Formal model for the specialized simulator.

$$x(t+1) = \mathrm{S}\left(\sum w_i x_i(t)\right) \qquad (1)$$

Here, xi(t) and x(t+1) are the input signal at the previous step and the output signal at the next step, respectively, and they are +1 and -1 for the firing and non-firing states respectively. wi is the synaptic connection strength, and it is positive and negative for the concordant and discordant synapses, respectively. S is a special step function that outputs +1 and -1 when the input is positive and negative, respectively.

The operation of the modified Hebbian learning can be approximately described using the following differential equation:

$$\frac{dw_i}{dt} = -\eta\left|x - x_i\right| \qquad (2)$$

Here, η is the changing speed of the synaptic connection strength and should be optimized to maximize the learning efficiency. We executed the numerical simulation for our network.

Figure 6 shows the synaptic connection strengths obtained after the simulation. It was confirmed that the network works as AND, OR, and XOR by these synaptic connection strengths. The neural network succeeded in learning multiple logics at least on the simulator.

5. Emulated experiment

Figure 7 shows the experimental method emulated using a FPGA and trimming resistors. We emulated the neurons using a FPGA and the synapses using the trimming resistors, connected them using a flat connector, applied Switch, In1, and In2 and measured Out using an oscilloscope.

Figure 8 shows the experimental results obtained using FPGA and trimming resistors. It was confirmed that the network works as AND, OR, and XOR by the abovementioned synaptic connection strengths. The neural network succeeded in learning multiple logics also on actual hardware.

6. Conclusion

We proposed a simplified architecture for a cellular neural network suitable for high-density integration of electron devices. A neuron consists of only eight transistors, and a synapse consists of just only one variable resistor. First, we developed a specialized simulator to estimate the practical operation. Moreover, we emulated the neural

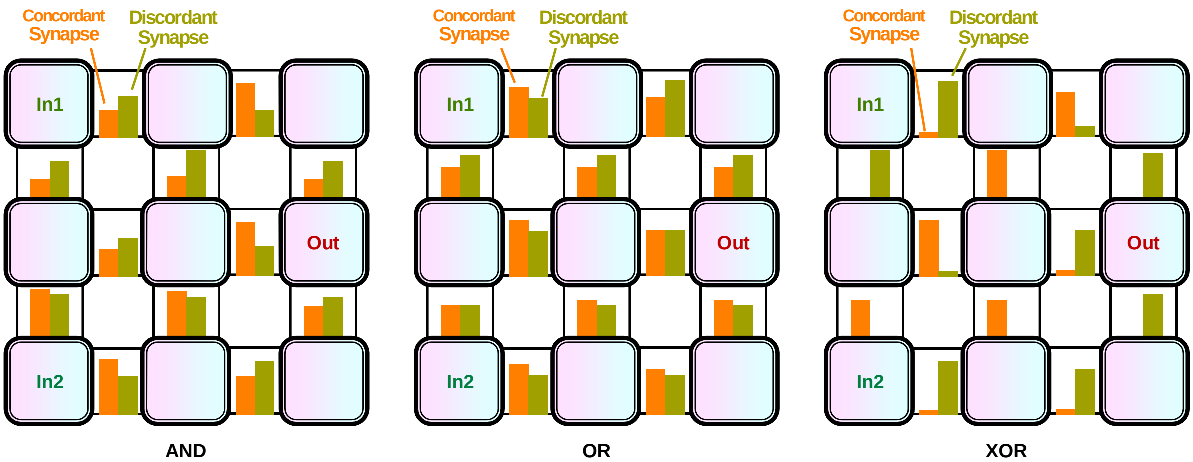

Fig. 6. Synaptic connection strengths obtained after the simulation.

network using a FPGA and trimming resistors. The neural network succeeded in learning multiple logics even in a small-scale network.

In this presentation, we emulated the neural network using a FPGA and trimming resistors. However, the same functions can be realized using integrated devices, such as LSI for the neuron and memristors or ferroelectric capacitors for the synapses. We would like to insist that the results obtained here can be surely obtained also using the integrated devices. Therefore, we think that this result indicates that our proposal has a big potential for future electronics using neural networks.

Acknowledgments

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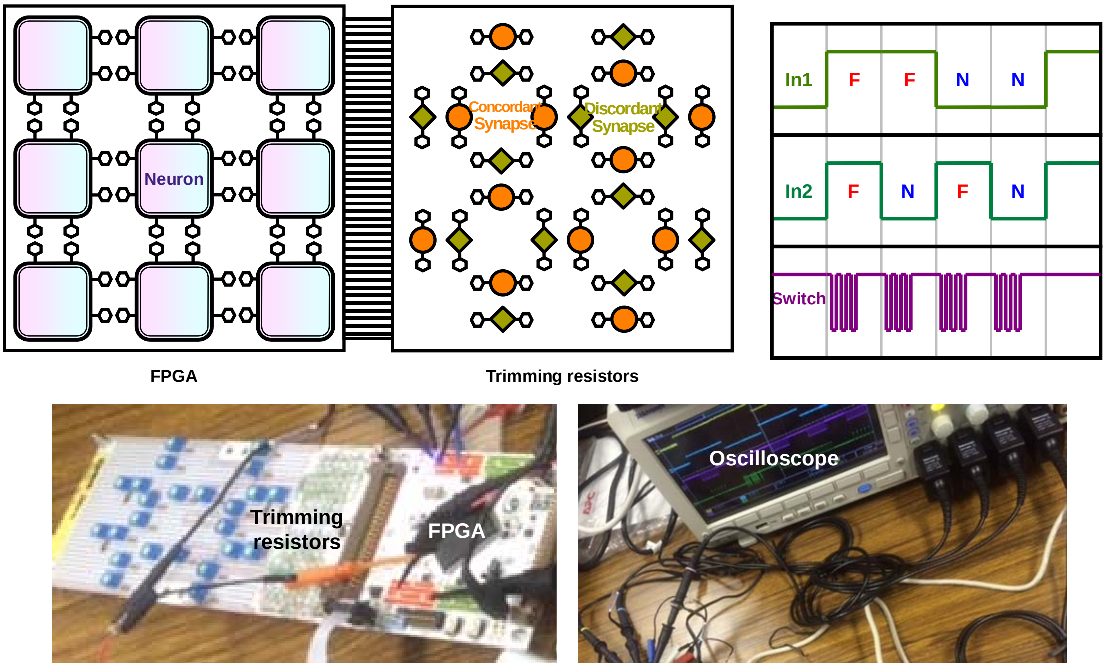

Fig. 7. Experimental method emulated using FPGA and trimming resistors.

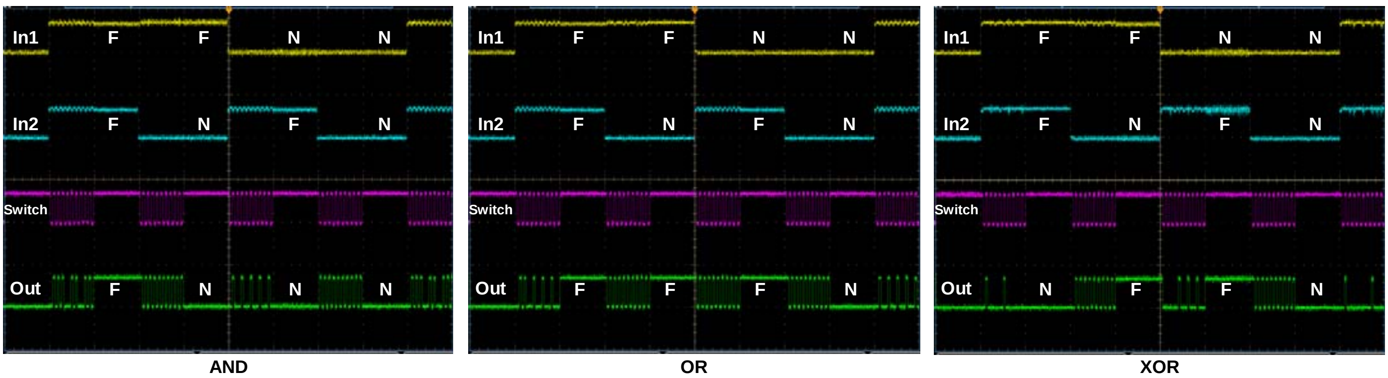

Fig. 8. Experimental results obtained using FPGA and trimming resistors.