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Analysis and Design of Class-DE Amplifier with Nonlinear Shunt Capacitances at Any Duty Ratio

Hiroo Sekiya† and Marian K. Kazimierczuk‡

†Graduate School of Advanced Integration Science, Chiba University
1-33, Yayoi-cho, Inage-ku, Chiba, 263-8522 Japan
‡Department of Electrical Engineering, Wright State University
3640 Colonel Glenn Highway Dayton, OH 45435, USA
Email: sekiya@faculty.chiba-u.jp, marian.kazimierczuk@wright.edu

Abstract—This paper presents an analytical expressions for the class-DE amplifier designs at any switch-on duty ratio, taking into account the nonlinear MOSFET drain-source parasitic capacitances. A design example along with PSPICE-simulation and experimental results indicate the validity of our analysis.

1. Introduction

The class-DE power amplifier [1]–[4] is one of the optimized class-D amplifiers, which satisfy both zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. Because of class-E ZVS/ZDS operation, the class-DE amplifier can operate with high power conversion efficiency at high operating frequencies.

Since class-E ZVS/ZDS should be satisfied with two conditions simultaneously, it is difficult to determine the element values of class-DE amplifiers. Therefore, several analyses were carried out to design it [1]–[4]. It is important to consider the nonlinearity of the shunt capacitances, which are the MOSFET parasitic output capacitance, under high-frequency operations, in particular [2]-[4]. The switch-on duty ratio is also one of the important parameters to design the class-DE amplifier. It is well known that large switch-on duty ratio provides high output power. Conversely, the maximum frequency of the class-DE amplifier becomes low as switch-on duty ratio increases. Most analyses carried out until now assume 25% switch-on duty ratio [1], [3], [4]. It is useful to derive the analytical expressions of the class-DE amplifier at any duty ratio, especially under high-frequency operations.

The purpose of this paper is to obtain the analytical expressions for the class-DE amplifier designs at any switch-on duty ratio, taking into account the nonlinear MOSFET drain-source parasitic capacitances of the diode junction. A design example along with PSPICE-simulation and experimental results indicate the validity of our analysis.

2. Class-DE amplifier

Figure 1 shows the circuit topology of the class-DE amplifier [1]-[4]. The elements L_f and C_0 realize a series-tuned circuit whose resonant frequency equals the operating frequency f. The element L causes the phase-shift of the output current. Figure 2 shows example waveforms of the class-DE amplifier for the nominal

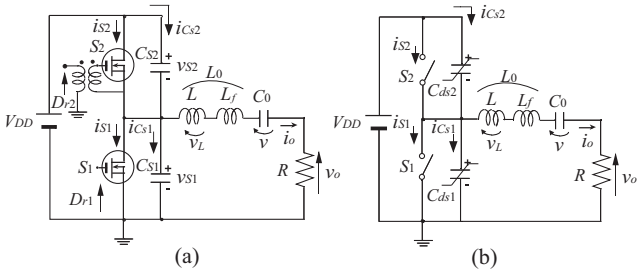

Figure 1: Class-DE amplifier. (a) Circuit topology. (b) Equivalent circuit.

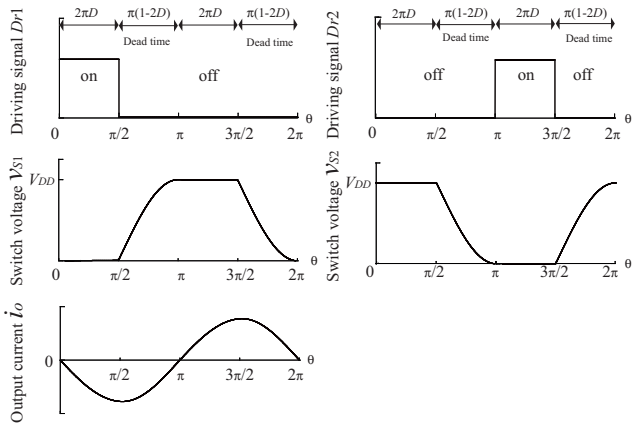

Figure 2: Nominal waveform of class-DE amplifier for D = 0.25.

operation. In the operation cycle of the class-DE amplifier, there are two dead-time intervals when both switches are OFF. During the dead-time intervals, the voltage across one of the switches decreases and reaches zero when the switch turns ON. Additionally, the slope of the voltage is also zero at turn-on instant, that is,

$$v_{S1}(2\pi) = 0, \qquad \left.\frac{dv_{S1}(\theta)}{d\theta}\right|_{\theta=2\pi} = 0, \tag{1}$$

$$v_{S2}(\pi) = 0, \qquad \left.\frac{dv_{S2}(\theta)}{d\theta}\right|_{\theta=\pi} = 0. \tag{2}$$

Table 1: Switching Pattern

Intervals	D_{r1}	D_{r2}
$0 \le \theta < 2\pi D$	ON	OFF
$2\pi D \le \theta < \pi$	OFF	OFF
$\pi \le \theta < \pi + 2\pi D$	OFF	ON
$\pi + 2\pi D \le \theta < 2\pi$	OFF	OFF

These conditions are called as the class-E zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. Because of the class-E ZVS/ZDS conditions, the switching power losses in the class-DE amplifier become zero. Therefore, the high power conversion efficiency can be achieved at high operating frequencies.

3. Waveform and Design Equations

3.1. Assumptions

The analysis in this paper is based on the following assumptions.

(a) The shunt capacitances consist of only the drain-source parasitic capacitances of the MOSFETs whose characteristic is expressed as

$$C_{ds} = \frac{C_{j0}}{\sqrt{1 + \dfrac{v_S}{V_{bi}}}}, \tag{3}$$

where v_S is the drain-to-source voltage, V_{bi} is the built-in potential, which typically ranges from 0.5 to 0.9 V, and C_{j0} is the capacitance at $v_S = 0$ [2], [3].

(b) Both MOSFETs are identical and are modeled as ideal switches and drain-source parasitic capacitances.

(c) All passive elements except shunt capacitances are linear elements and do not have parasitic resistances.

(d) The loaded quality factor of the resonant filter $Q = \omega L_0/R$ is high enough to generate nearly pure sinusoidal output current. The current through the $L_f - C_0$ circuit and the load resistance is sinusoidal at the operating frequency f,

$$i_o = I_m \sin(\theta + \varphi), \tag{4}$$

where $\theta = \omega t = 2\pi f t$ represents the angular time.

(e) The switching pattern is the same as that given in Table 1.

(f) At the end of the dead time, both the switch voltages v_{S1} and v_{S2} satisfy class-E ZVS/ZDS conditions.

Under the above assumptions, the equivalent model of the class-DE amplifier can be obtained as shown in Fig. 1(b).

3.2. Voltage Waveforms

The analysis for steady state is performed in the interval $0 \le \theta < 2\pi$. The following relation between v_{S1} and v_{S2} is always valid:

$$\frac{v_{S1}(\theta)}{V_{DD}} = 1 - \frac{v_{S2}(\theta)}{V_{DD}}. \tag{5}$$

The slope of the switch voltage v_{S1} is expressed as

$$\frac{dv_{S1}(\theta)}{d\theta} = \frac{-I_m}{\omega(C_{ds1} + C_{ds2})} \sin(\theta + \varphi). \tag{6}$$

From the class-E ZDS condition for v_{S1} in (1), we obtain $\varphi = 0$ and π. In this paper, we consider that the amplitude of the output current I_m is positive. Therefore, the phase difference is determined as

$$\varphi = \pi. \tag{7}$$

Similarly, (7) is valid for the class-E ZDS condition for v_{S2}. For $0 \le \theta < 2\pi$, the switch S_1 is on and the switch S_2 is off. Therefore, the switch voltages are constant,

$$v_{S1}(\theta) = 0, \quad v_{S2}(\theta) = V_{DD}. \tag{8}$$

From (3), (6), and $v_{S1}(2\pi D) = 0$, we obtain

$$\begin{aligned} &2\omega C_{j0} V_{bi} \left[\sqrt{1 + \frac{v_{S1}}{V_{bi}}} - \sqrt{1 + \frac{V_{DD} - v_{S1}}{V_{bi}}} \right. \\ &\left. + \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right] = I_m[\cos(2\pi D) - \cos\theta]. \end{aligned} \tag{9}$$

The switch voltages are $v_{S1}(\pi) = V_{DD}$ and $v_{S2} = 0$ because of the class-E ZVS condition in (2). By substituting $\theta = \pi$ and $v_{S1} = 0$, the amplitude I_m is

$$I_m = \frac{4\omega C_{j0} V_{bi} \left[\sqrt{1 + \dfrac{V_{DD}}{V_{bi}}} - 1 \right]}{1 + \cos(2\pi D)}. \tag{10}$$

From (9) and (10), we have

$$\begin{aligned} &\sqrt{1 + \frac{V_{DD}}{V_{bi}} \frac{v_{S1}}{V_{DD}}} - \sqrt{1 + \frac{V_{DD}}{V_{bi}} - \frac{V_{DD}}{V_{bi}} \frac{v_{S1}}{V_{DD}}} \\ &+ \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \\ &- \frac{2[\cos(2\pi D) - \cos\theta] \left[\sqrt{1 + \dfrac{V_{DD}}{V_{bi}}} - 1 \right]}{1 + \cos(2\pi D)} = 0. \end{aligned} \tag{11}$$

We can solve (11) for v_{S1} analytically,

$$\begin{aligned} \frac{v_{S1}(\theta)}{V_{DD}} &= \frac{1}{2} \pm \frac{1}{2} \left\langle 1 - 4 \left(\frac{V_{bi}}{V_{DD}} \right)^2 \left\{ -1 - \frac{V_{DD}}{V_{bi}} \right. \right. \\ &+ \left[1 + \frac{V_{DD}}{2V_{bi}} - \frac{1}{2} \left(2 \left(1 - \sqrt{1 + \frac{V_{DD}}{V_{bi}}} \right) \right. \right. \\ &\left. \left. \times \frac{\cos(\theta) - \cos(2\pi D)}{1 + \cos(2\pi D)} + 1 - \sqrt{1 + \frac{V_{DD}}{V_{bi}}} \right)^2 \right]^2 \left. \left. \right\} \right\rangle^{\frac{1}{2}}, \end{aligned} \tag{12}$$

where the sign "$\pm$" of the second term on the right-hand side changes at the boundary of $v_{S1}/V_{DD} = 1/2$. Namely, the sign is '$-$' for $2\pi D \le \theta < \cos^{-1}([1-\cos(2\pi D)]/2)$ and '$+$' for $\cos^{-1}([1-\cos(2\pi D)]/2) \le v_{S1} < \pi$.

For $\pi \le \theta < \pi + 2\pi D$, the switch voltages and currents have the following relationships because of the symmetry of the operation of the switches,

$$v_{S1}(\theta) = v_{S2}(\theta - \pi), \quad v_{S2}(\theta) = v_{S1}(\theta - \pi). \tag{13}$$

3.3. DC Supply Current and Output Voltage, Current, and Power

The dc supply current I_D is given as the average of the supply current flowing from the dc voltage source V_{DD},

$$\begin{aligned} I_D &= \frac{1}{2\pi}\int_0^{2\pi} [i_{S2}(\theta) + i_{CS2}(\theta)]\, d\theta \\ &= \frac{2\omega C_{j0} V_{bi}\left[\sqrt{1+\dfrac{V_{DD}}{V_{bi}}} - 1\right][1-\cos(2\pi D)]}{\pi[1+\cos(2\pi D)]}. \end{aligned} \tag{14}$$

Note that the average value of the current through the shunt capacitance i_{C2} means the amount of charging/discharging electric charge. Therefore, it is always zero. From (10) and (14), the normalized amplitude of the output current is expressed as

$$\frac{I_m}{I_D} = \frac{2\pi}{1-\cos(2\pi D)}. \tag{15}$$

Using (15), we obtain the dc supply power as

$$P_{dc} = V_{DD} I_D = \frac{I_m V_{DD}[1-\cos(2\pi D)]}{2\pi}. \tag{16}$$

The output power P_o is given by

$$P_o = \frac{I_m V_m}{2} = \frac{R I_m^2}{2} = \frac{V_m^2}{2R}, \tag{17}$$

Ideally, the power conversion efficiency of the class-DE amplifier is 100% on the nominal operation,

$$P_{dc} = P_o. \tag{18}$$

From (16), (17), and (18), we can obtain the amplitude of the output voltage normalized with respect to the dc supply voltage as

$$\frac{V_m}{V_{DD}} = \frac{1-\cos(2\pi D)}{\pi}. \tag{19}$$

Figure 3(a) shows the normalized amplitudes of the output current as a function of the switch-on duty ratio D.

From (17) and (19), we have

$$P_o = \frac{R I_m^2}{2} = \frac{V_m^2}{2R} = \frac{V_{DD}^2[1-\cos(2\pi D)]^2}{2R\pi^2}. \tag{20}$$

Figure 3(b) shows the normalized output power as a function of the switch-on duty ratio. It is seen from Fig. 3(b) that the output power increases as the switch-on duty ratio increases.

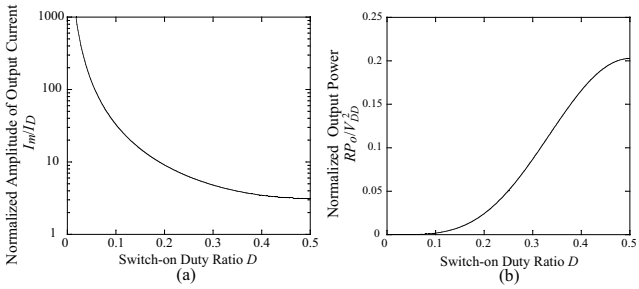

Figure 3: Normalized output current and voltage as a function of the switch-on duty ratio D. (a) Normalized output current I_m/I_D. (b) Normalized output power RP_o/V_{DD}^2

3.4. Voltage Across the Load Reactance

The fundamental component of the voltage $v_L(\theta)$ across the reactance L is expressed as

$$v_L(\theta) = V_L(-\cos\theta), \tag{21}$$

where

$$V_L = \omega L I_m. \tag{22}$$

From (22) and $V_m = RI_m$, we obtain

$$\frac{V_L}{V_m} = \frac{\omega L}{R}. \tag{23}$$

The normalized magnitude V_L/V_{DD} is derived from the Fourier integral

$$\frac{V_L}{V_{DD}} = \frac{1}{\pi}\int_0^{2\pi} \frac{v_{S1}(\theta)}{V_{DD}}(-\cos\theta)d\theta. \tag{24}$$

(24) can be solved numerically. Here, the function $H(m, V_{DD}/V_{bi}, D)$ is defined as

$$H \equiv \frac{V_L}{V_{DD}} = \frac{1}{\pi}\int_0^{2\pi} \frac{v_{S1}(\theta)}{V_{DD}}(-\cos\theta)d\theta. \tag{25}$$

Figure 4 shows plots of the function H. In order to illustrate Fig. 4(a), the trapezoidal rule with $2\pi/10000$ of time-step of θ is used to calculate the integration of (24).

3.5. Design Equations

From (20), the load resistance R is given as

$$R = \frac{V_{DD}^2[1-\cos(2\pi D)]^2}{2\pi^2 P_o}. \tag{26}$$

From the definition of the loaded-quality factor Q, the inductance L_0 is given as

$$L_0 = \frac{QR}{\omega} = \frac{QR}{2\pi f}. \tag{27}$$

From (19), (23), and (25), the inductance L is

$$L = \frac{\pi R H}{2\pi f(1-\cos(2\pi D))}. \tag{28}$$

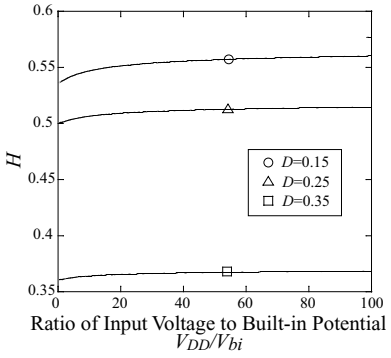

Figure 4: Plots of the function H as a function of V_{DD}/V_{bi}

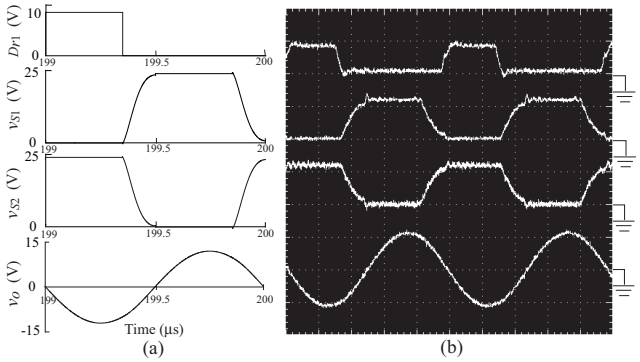

Figure 5: Waveforms by PSPICE simulation and circuit experiment. (a) PSPICE-simulated waveforms. (b) Experimental waveforms. Vertical: D_{r1}: 10 V/div, v_{S1} and v_{S2}: 20 V/div, and v_o: 10 V/div. Horizontal: 200 ns/div.

From (27) and (28), the inductance L_f is obtained as

$$L_f = L_0 - L = \frac{R}{2\pi f}\left[Q - \frac{\pi H}{1-\cos(2\pi D)}\right]. \qquad (29)$$

The identical resonant filter with the resonant frequency $f = \omega/2\pi$ is realized by L_f and C_0. From $f = 1/(2\pi\sqrt{L_f C_0})$ and (29), the resonant capacitance C_0 is expressed analytically as

$$C_0 = \frac{1}{2\pi f R\left[Q - \dfrac{\pi H}{1-\cos(2\pi D)}\right]}. \qquad (30)$$

In these design equations, we need numerical calculations for obtaining H, which is used for the derivation of C_0 in (30).

4. Design Example and Experimental Verification

The design example with the discrete MOSFET devices is given. The design specifications are: operating frequency $f = 1$ MHz, dc supply voltage $V_{DD} = 24$ V, output resistance $R = 50\ \Omega$, and loaded quality factor $Q = 8$.

Table 2: Analytical Predictions and Experimental Measurements

	Calculated	Measurement	Difference
f	1 MHz	1.02 MHz	2.0%
V_{DD}	24 V	24 V	0.0%
D	0.35	0.35	0.0%
C_0	427 pF	424 pF	-0.7%
L_0	63.6 μH	62.0 μH	-2.5%
R	50 Ω	49.8 Ω	-0.6%
Q	8	7.98	-0.3 %
P_o	1.46 W	1.32 W	-10.6 %

It is considered that the IRF 530 MOSFETs are used as the switching devices. The values of grading coefficient m, the built-in potential V_{bi}, and C_{j0} of IRF530 MOSFET are obtained as $V_{bi} = 0.8$V and $C_{j0} = 1.03$ nF from the PSPICE model. From (10) and (20), the duty ratio D is obtained as $D = 0.35$. Therefore, $L_0 = 63.6\ \mu$F is obtained from (27). From the numerical calculations of (25), H is 0.366. Therefore, the resonant capacitance C_0 is 427 pF from (30).

Figure 5 shows the PSPICE-simulated waveforms and the experimental waveforms. From Fig. 5, it can be confirmed that both the PSPICE-simulated waveforms and the experimental waveforms satisfy the class-E ZVS/ZDS conditions. Table 2 gives the analytical predictions and experimental measurements. From this table, it is seen that the experimental measurements agreed with the analytical predictions quantitatively. The results in Figure 5 and Table 2 indicate the validity of the analytical expressions in this paper. The laboratory measurements showed the 95.7% power conversion efficiency with 1.3 W output power.

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