2010 International Symposium on Nonlinear Theory and its Applications
NOLTA2010, Krakow, Poland, September 5-8, 2010

Forced Chaos Generator with CMOS Variable Active Inductor Circuit

Yusuke Tsubaki†, Munehisa Sekikawa‡, and Yoshihiko Horio†,‡

†Graduate School of Engineering, Tokyo Denki University, 2-2 Kanda-Nishiki-cho, Chiyoda-ku, Tokyo 101-8457, Japan
‡Aihara Innovative Mathematical Modelling Project, FIRST, JST,
IIS, the University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
E-mail: 09kme35@ms.dendai.ac.jp, sekikawa@sat.t.u-tokyo.ac.jp, horio@eee.dendai.ac.jp

Abstract—We propose a forced chaos generator with a CMOS variable active inductor circuit. The equivalent inductance of the variable active inductor in the proposed circuit can be controlled by an external voltage. The oscillation frequency of the circuit can be tuned by applying an external signal. We then realize the folding-and-stretching mechanism of chaotic motion by applying a periodic external signal. The chaotic dynamics are confirmed through SPICE simulations with TSMC 0.35 μm CMOS semiconductor process parameters. Moreover, we present bifurcation phenomena, which are generated when the amplitude and the period of the external signal are changed as bifurcation parameters.

1. Introduction

Chaotic phenomena observed in electronic circuits have been extensively investigated. It is well known that chaos, torus, and frequency entrainment occur in non-autonomous circuits for certain values of the amplitude and period of the external signal [1]. In addition, autonomous chaotic circuits such as the double scroll circuit [2],[3] and the hysteresis chaotic circuit [4] have also been proposed. Recently, researchers have attempted to apply chaos to real-world problems such as chaotic communication, chaotic encryption, and combinatorial optimization problems. For these applications, IC implementation is necessary because miniaturization, high-speed operation, and large-scale integration of the chaotic circuits are essential. Against this background, several chaotic circuits have been implemented as integrated circuits [5]-[7].

As one of these chaotic circuits, a three-dimensional autonomous chaotic circuit, based on a change in the oscillation frequency, has been proposed (Fig. 1) [8]. This circuit consists of a linear negative conductance, a capacitor C, two inductors L_1 and L_2, and a diode D. By replacing the diode D in the circuit with a current-controlled switch, the sub-circuit consisting of L_1, L_2, and D can be treated as a variable nonlinear inductor. The oscillation frequency of the circuit is changed by the switching operation of the diode. Therefore, this effect causes a stretching-and-folding mechanism, which is the basic mechanism of the chaos generation.

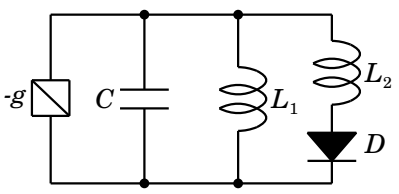


Figure 1: Three-dimensional autonomous chaotic circuit proposed in Ref. [8].

In this paper, we propose a forced chaos generator based on the circuit in Fig. 1 with a CMOS variable active inductor circuit. The equivalent inductance of the variable active inductor in the proposed circuit can be controlled by the external voltage. We change the oscillation frequency of the circuit by applying a periodic external signal to the variable active inductor. Based on the above principle, the above-mentioned folding-and-stretching mechanism is realized. We confirm the chaotic dynamics of the proposed circuit through SPICE simulations with TSMC 0.35 μm CMOS semiconductor process parameters. Moreover, we present bifurcation phenomena, which are generated when the amplitude and period of the external signal are changed as bifurcation parameters.

2. Forced Chaos Generator with CMOS Variable Active Inductor Circuit

Figure 2 shows the forced chaos generator with a CMOS variable active inductor circuit. First, we focus on the CMOS variable active inductor and omit C_3 from the circuit in the figure.

We assume that $C \equiv C_1 = C_2$ and $R \equiv R_1 = R_2$.

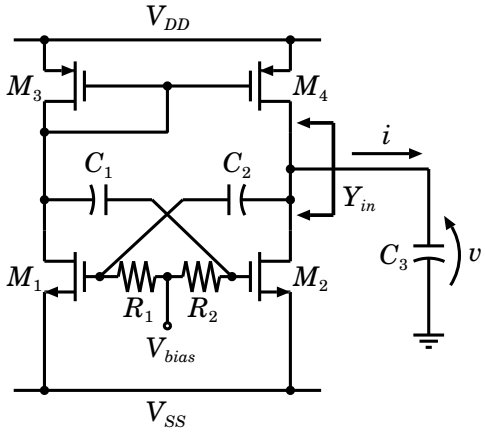


Figure 2: Forced chaos generator with CMOS variable active inductor circuit.

Table 1: Coefficients in Eqs. (2) and (3).

a_0	$g_{dsn} + g_{dsp}$
a_1	$a_0^2 + 2a_0 g_{mp} - g_{mn}g_{mp} + g_{mp}^2 + a_0 g_{mn}g_{mp}R + g_{mn}^2 g_{mp}R - g_{mn}g_{mp}^3 R$
a_2	$C^2\{1 + (a_0 + g_{mp})R\}[1 + R\{a_0 + g_{mp} - g_{mn}(g_{mn} + g_{mp})R\}]$
a_3	$C(a_0 + g_{mp})(a_0 + g_{mp} - g_{mn}g_{mp}R)$
a_4	$C^3\{1 + 2(a_0 + g_{mp})R + (a_0 - g_{mn} + g_{mp})(a_0 + g_{mn} + g_{mp})R^2 - g_{mn}(a_0 + g_{mp})(2g_{mn} + g_{mp})R^3\}$
b	$a_0 + g_{mp} + C^2R\{1 + (a_0 + g_{mp})R\}\omega^2$

We also assume that each of the two NMOSFETs and two PMOSFETs match perfectly, and operate on equal dc currents: that is, $g_{mn} \equiv g_{m1} = g_{m2}$, $g_{mp} \equiv g_{m3} = g_{m4}$, $g_{dsn} \equiv g_{ds1} = g_{ds2}$, and $g_{dsp} \equiv g_{ds3} = g_{ds4}$. The input admittance Y_{in} of the CMOS variable active inductor is derived as

$$Y_{in} = G + jB, \tag{1}$$

where

$$G = a_0 + \frac{C^2R\omega^2(a_1 + a_2\omega^2)}{b^2 + C^2\omega^2} \tag{2}$$

and

$$B = \frac{a_3\omega + a_4\omega^3}{b^2 + C^2\omega^2}. \tag{3}$$

a_0, a_1, a_2, a_3, a_4, and b are given in Table 1. When $G < 0$ and $B < 0$ in Eq. (1), the input admittance of the CMOS variable active inductor consists of negative conductance and inductive susceptance connected in parallel. In this case, the equivalent inductance L_{eq} of the circuit is expressed as

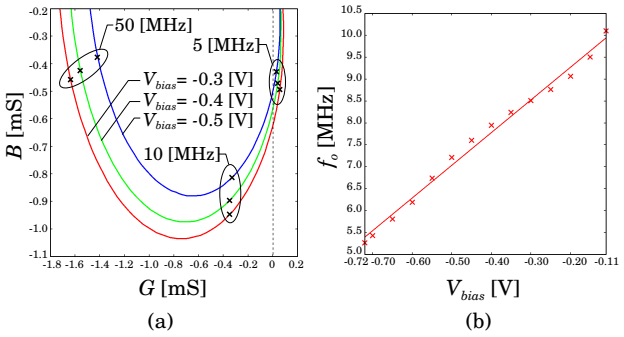
$$L_{eq} = -\frac{1}{\omega B} = -\frac{b^2 + C^2\omega^2}{a_3\omega^2 + a_4\omega^4}. \tag{4}$$

Figure 3(a) shows the admittance chart of the CMOS variable active inductor circuit obtained from SPICE simulations with TSMC 0.35 μm CMOS process parameters. As shown in Fig. 3(a), the value of L_{eq} can be controlled by the external voltage V_{bias}. Table 2 lists the circuit parameters used in the SPICE simulations.

In addition, a periodic solution can be generated by connecting C_3 to the CMOS variable active inductor circuit in parallel, because the CMOS variable active inductor circuit

Table 2: Circuit parameters.

Element	Value
W/L of M_1, M_2	7.2/0.6 μm
W/L of M_3, M_4	6.6/0.6 μm
R_1, R_2	5 kΩ
C_1, C_2	3 pF
C_3	10 pF
V_{DD}	1.65 V
V_{SS}	−1.65 V



(a) (b)

Figure 3: (a) Admittance chart of the CMOS variable active inductor circuit. (b) Oscillation frequency of periodic solutions as a function of V_{bias}.

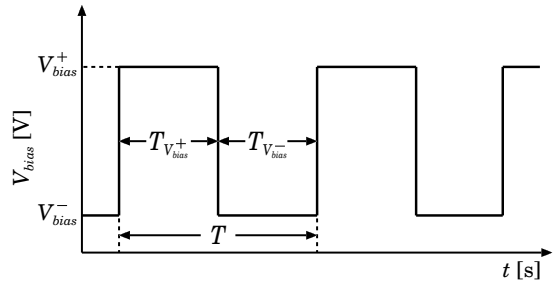


Figure 4: External periodic signal for V_{bias}.

has negative conductance in a certain frequency range. The oscillation frequency f_o of the periodic solution is almost equal to the resonance frequency $1/(2\pi\sqrt{L_{eq}C_3})$. Thus, we can change the oscillation frequency of the periodic solution by tuning V_{bias}. As obtained from the SPICE simulations, Fig. 3(b) shows the oscillation frequency of the periodic solution as a function of V_{bias}.

On the basis of the above-mentioned principle, we change the oscillation frequency of the circuit by applying a periodic external voltage, shown in Fig. 4 as V_{bias}. As a result, the forced chaos generator based on the circuit in Fig. 1 is realized.

3. SPICE Simulations

We observe v and i (Fig. 2) by varying the amplitude and period of the external periodic signal as shown in Fig. 4. We assume that $T_{V_{bias}^+} = T/2$ and $T_{V_{bias}^-} = T/2$. Figure 5 shows a typical chaotic attractor on the $v - i$ plane with $T = 100$ ns, $V_{bias}^+ = -0.11$ V, and $V_{bias}^- = -0.72$ V. In addition, in order to examine the properties of the orbits, we define the Poincaré sections of Fig. 5 at certain phases

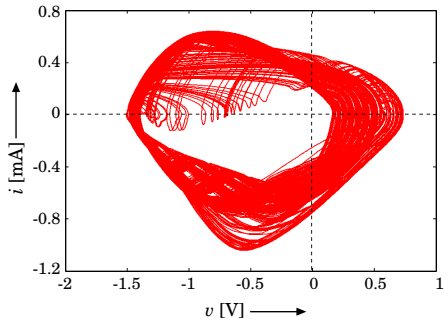


Figure 5: Chaotic attractor on $v-i$ plane obtained by SPICE simulation ($V^+_{bias} = -0.11$ V and $V^-_{bias} = -0.72$ V).

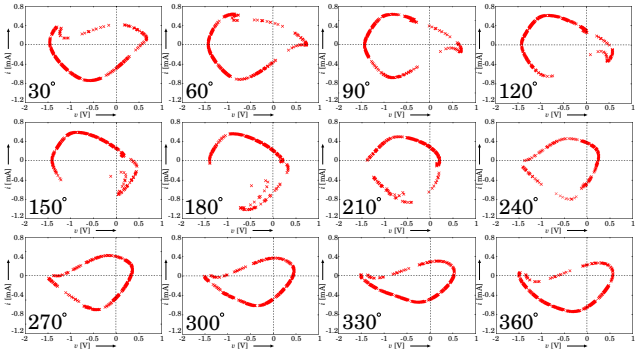


Figure 6: Poincaré sections of attractors in Fig. 5. Values indicate phases of the section.

of the external periodic signal as shown in Fig. 6. From this figure, we can confirm that the attractor in Fig. 5 is chaotic, because a folding-and-stretching mechanism is observed.

Bifurcation phenomena are observed when the amplitude and period of the external signal are swept as bifurcation parameters. In the following, we define the Poincaré section at each rising edge of the external square waveform.

Figure 7 shows the observed attractors and their Poincaré sections. The amplitude parameters of the external signal are fixed at $V^+_{bias} = -0.11$ V and $V^-_{bias} = -0.72$ V. The period T of the external signal is varied. Here, we define a number of points on the Poincaré section as the period. For example, we can see 5 points in Fig. 7(a.2); therefore, the period of the attractor in Fig. 7(a.1) is 5. Figure 8 shows a bifurcation diagram of the attractor on the Poincaré section when the period T of the external signal is swept. As T is increased, the period-5 orbit bifurcates and a period-10 orbit is generated, as shown in Fig 7(b). In Fig. 8, a period-doubling route to chaos can be seen for $72.5 < T < 75.5$. Unfortunately, the limited calculation precision of the SPICE simulations prevents solutions with periods greater than 20 from being observed.

Figure 9 shows the bifurcation phenomena when V^+_{bias} of the external signal is changed (Fig. 4). In the figure, the horizontal axis and the vertical axis are V^+_{bias} and v of the attractors on the Poincaré sections, respectively. The period and lower voltage of the external signal are fixed at $T = 100$ ns and $V^-_{bias} = -0.72$ V, respectively. As shown in

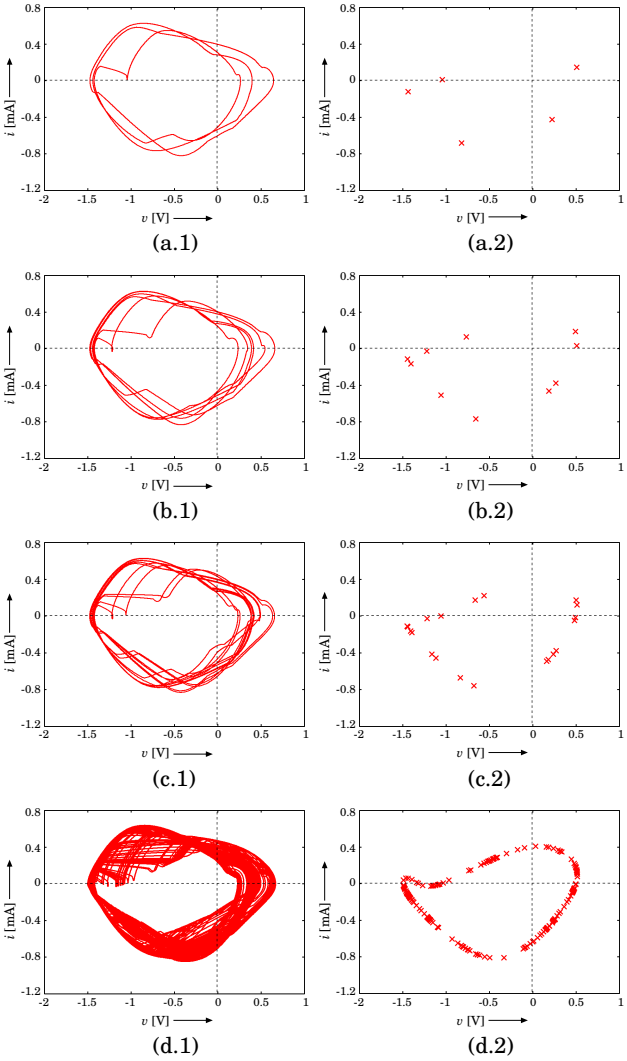


Figure 7: Attractors and their Poincaré sections. (a) Period-5 ($T = 74.5$ ns), (b) Period-10 ($T = 74.9$ ns), (c) Period-20 ($T = 75.2$ ns), and (d) Chaotic attractor ($T = 75.4$ ns).

Fig. 9, period-adding phenomena [9], [10] are observed.

To understand the properties of the complex attractors in the region between periodic solutions, we examine the attractors on the Poincaré sections at various phases of the external signal. Between $V^+_{bias} = -0.8$ V and $V^+_{bias} = -0.3$ V in Fig. 9, all of the attractors on the Poincaré sections asymptotically converge to closed curves. This confirms that the observed complex attractors in the range of -0.8 V$< V^+_{bias} <-0.3$ V in Fig. 9 are quasi-periodic attractors. Moreover, we conclude that when $V^+_{bias} > -0.2$ V, the observed complex attractors are chaotic because a folding-and-stretching mechanism is observed. Therefore, the bifurcation phenomenon in Fig. 9 is the chaos via torus breakdown [9]. The border between chaos and torus exists around $V^+_{bias} = -0.3$ V.

Furthermore, we consider the case where the duty ratio of the periodic external signal $T_{V^+_{bias}}/T$ is varied. Figure 10 shows the bifurcation diagram in which $T_{V^+_{bias}}/T$ is swept as

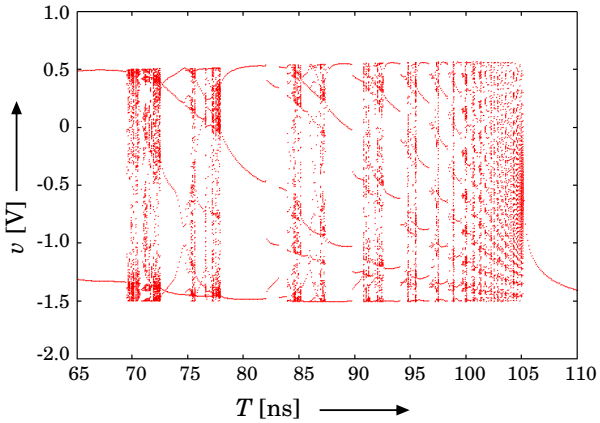


Figure 8: Bifurcation diagram when T is swept as bifurcation parameter ($V^+_{bias} = -0.11$ V and $V^-_{bias} = -0.72$ V).

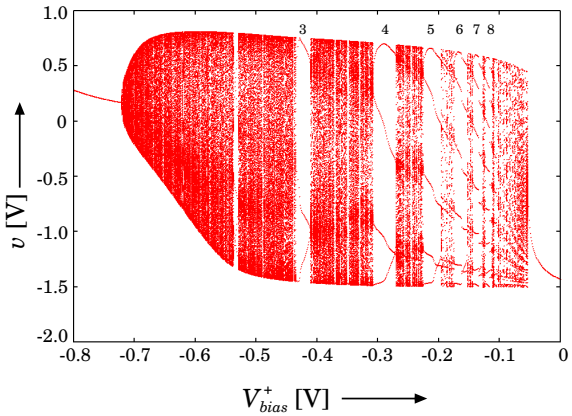


Figure 9: Bifurcation diagram when V^+_{bias} is swept as bifurcation parameter ($V^-_{bias} = -0.72$ V and $T = 100$ ns).

the bifurcation parameter. The horizontal axis of the figure is the duty ratio of the external signal in percent, and the vertical axis is v of the attractors on the Poincaré sections. Here, $V^+_{bias} = -0.11$ V, $V^-_{bias} = -0.72$ V, and $T = 100$ ns. To understand the properties of the complex attractors in Fig. 10, we examine the attractors on the Poincaré sections at various phases of the external signal. As a result, we observed the folding-and-stretching mechanism; thus, the complex orbits in Fig. 10 are chaotic.

4. Conclusions

We have proposed a forced chaos generator with a CMOS variable active inductor circuit. Chaos, a quasi-periodic attractor, and a periodic attractor were observed in SPICE simulations. Poincaré section analyses were used to confirm the chaotic dynamics of the proposed circuit. Moreover, we presented the bifurcation phenomena when the amplitude and period of the external signal were swept as bifurcation parameters. As a future task, we plan to develop the proposed circuit for practical IC implementation.

This research was supported in part by JSPS through its Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program). This work was also supported by Kakenhi (20300085), and VDEC, the University of Tokyo in collaboration with Cadence Design Systems, Inc.

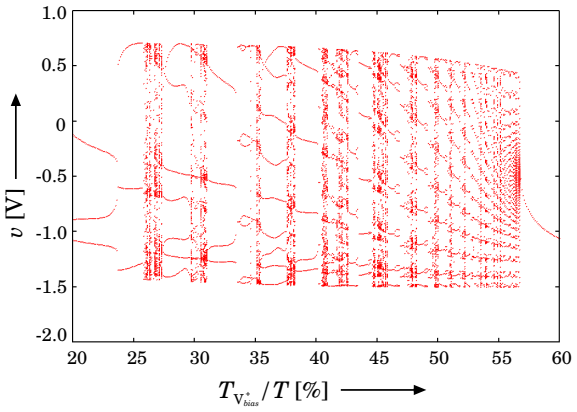


Figure 10: Bifurcation diagram when $T_{V^+_{bias}}/T$ is swept as bifurcation parameter ($V^+_{bias} = -0.11$ V, $V^-_{bias} = -0.72$ V, and $T = 100$ ns).

References

[1] N. Inaba and S. Mori, "Chaos via torus breakdown in a piecewise-linear forced van der Pol oscillator with a diode," *IEEE Trans. Circuits Syst.*, vol. 38, no. 4, pp. 398–409, 1991.

[2] T. Matsumoto, L. O. Chua, and M. Komuro, "The double scroll," *IEEE Trans. Circuits Syst.*, vol. CAS-32, no. 8, pp. 797–818, 1985.

[3] M. Shinriki M. Yamamoto, and S. Mori, "Multimode oscillations in a modified van der Pol oscillator containing a positive nonlinear conductance," *Proc. IEEE*, vol. 69, pp. 394–395, 1981.

[4] M. Kataoka and T. Saito, "A two-port VCCS chaotic oscillator and quad screw attractor," *IEEE Trans. Circuits Syst. I*, vol. 48, no. 2, pp. 221–225, 2001.

[5] T. Fujiwara, Y. Horio, and K. Aihara, "An integrated multi-scroll circuit with floatinggate MOSFETs," in *Proc. IEEE ISCAS*, vol. 3, pp. III-180–III-183, 2003.

[6] T. Hamada, M. Sekikawa, Y. Horio, and K. Aihara, "IC implementations of Shinriki's and Inaba's chaotic circuits," in *Proc. NOLTA*, pp. 1057–1070, 2006.

[7] T. Hamada, Y. Horio, and K. Aihara, "An IC implementation of a hysteresis two-port VCCS chaotic oscillator," in *Proc. ECCTD*, pp. 926–929, 2007.

[8] N. Inaba and S. Mori, "Chaotic phenomena in a circuit with a diode due to the change of oscillation frequency," *IEICE Trans. Fundamentals*, vol. E71, no. 9, pp. 842–849, 1988.

[9] T. Matsumoto, L. O. Chua, and R. Tokunaga, "Chaos via torus breakdown," *IEEE Trans. Circuits Syst.*, vol. 34, no. 3, pp. 240–253, 1987.

[10] L. O. Chua, Y. Yao, and Q. Young, "Devil's staircase route to chaos in a nonlinear circuit," *Int. J, Circuit Theory App.*, vol. 14, no. 4, pp. 315–329, 1986.