2010 International Symposium on Nonlinear Theory and its Applications
NOLTA2010, Krakow, Poland, September 5-8, 2010

Digital-Signal-Waveform Improvement for High-Speed VLSI Packaging

Moritoshi Yasunaga†, Hiroshi Nakayama†, Yuki Shimauchi†, and Ikuo Yoshihara‡

†Graduate School of Systems and Information Engineering, University of Tsukuba
Tsukuba, Ibaraki, 305-8573 JAPAN
‡Faculty of Engineering, Miyazaki University,
Gakuen Kibanadai Nishi, Miyazaki, 889-2192, Japan
Email: yasunaga@islab.cs.tsukuba.co.jp,{nakayama, shimauchi}@islab.cs.tsukuba.co.jp, yoshiha@cs.miyazaki-u.ac.jp

Abstract– Digital-signals propagating in the PCB traces are being distorted seriously causing system failures as the clock-frequency increases. And it is getting difficult to improve the distortions with conventional impedance-matching technique as the clock frequency increases to GHz, which is called "Signal-Integrity (SI) problem in the GHz era". In order to overcome this problem, we have already proposed a novel PCB-trace structure called "Segmental Transmission Line (STL)", which is designed using the genetic algorithms. In this paper, we develop a 250MHz-scale-up prototype of the STL and show effectiveness of the STL by measuring the signals propagating in the prototype.

1. Introduction

Digital-signal waveforms in PCBs (Printed Circuit Boards) have been distorted gradually since the clock-frequency got into the 100MHz-era. And in the GHz-era, the waveform distortion is one of the most serious problems in the PCB design for the VLSI packaging.

The waveform-distortion problem, or the so-called "the Signal-Integrity problem," comes from the fact that the PCB traces (wires) behave as transmission lines as their lengths are approaching the wavelengths of the digital signals propagating on them (e.g., the base-wave-length of 1GHz digital-signal in the PCB is about 15cm). The transmission line generates reflection waves, or noises at characteristic-impedance Z mismatched points, and the noises degrade the waveform terribly.

In the GHz-domain (from about 500MHz, precisely), however, the conventional Z-matching designs will not do their work gradually, and new techniques for the waveform-distortion have been craved in the GHz-era.

In order to overcome this difficulty, we have already proposed a novel transmission line called "Segmental Transmission Line (STL)", which is designed based on the genetic algorithms (GAs). And we have already shown its fundamental effectiveness theoretically and experimental-results using low-frequency prototypes [1][2][3].

In this paper, we show the STL design placing the focus on the genetic algorism and also show the experimental results on the recently developed 250MHz-STL scale-up prototype.

2. Segmental Transmission Line

No waveform distortion occurs in the PCB traces if nothing is connected to them as shown in the upper figure in Fig. 1. However, if some devices, e.g., VLSIs, are connected to the traces, their inputs, which can be regarded as load capacitances, cause characteristic-impedance mismatching and distort the signals terribly as shown in the lower figure in Fig. 1.

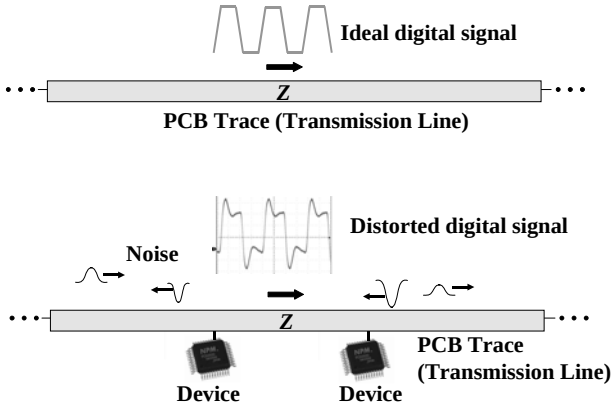


Fig. 1 Digital Signal Propagation and Distortion.

In the STL, a transmission line is divided into multiple (N) segments of individual characteristic impedance Z_i as shown in Fig. 2. And each Z_i is adjusted to achieve an ideal digital waveform at target points such as input-points to the LSIs on the line by superposing reflection waves generated at the interfaces between adjacent segments Z_i and Z_{i+1}. The adjustment of all Z_is however, results in a combinatorial-explosion-problem because the search-space expands to n^m, where n is the impedance range and m is the number of segments and it comes to 100^{10}-order usually. We have proposed to apply the genetic algorithms (GAs) to solve this problem and have already shown its effectiveness [1][2][3].

Figure 3 shows a bird-eye view and a cross-sectional view of the STL in the PCB. Characteristic impedance Z is a function of trace width W, trace thickness T, and insulator thickness D. In the STL, Z is thus controlled easily by adjusting W.

The STL structure can be easily and well mapped onto the chromosome of one-dimensional array of genes as shown in the upper figure in Fig. 4. This chromosome is called "Simple Chromosome". In the STL, each

segment-length L_i can be also used as a parameter, which expands the search-space more widely to include better solutions as shown in the lower figure in Fig. 3. The chromosome composed of both characteristic impedance Z_i and segment-length L_i is called "Hybrid Chromosome". In this variable-length-segment approach, however, we have to be careful not to produce fatal genes under the constraint that the total length is fixed.

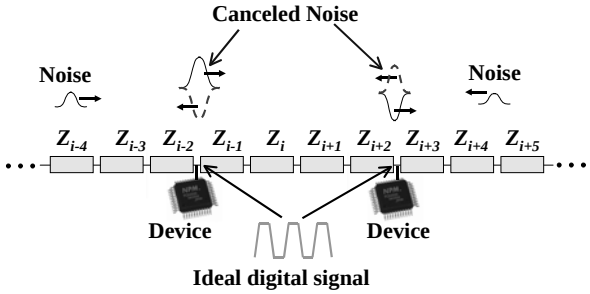
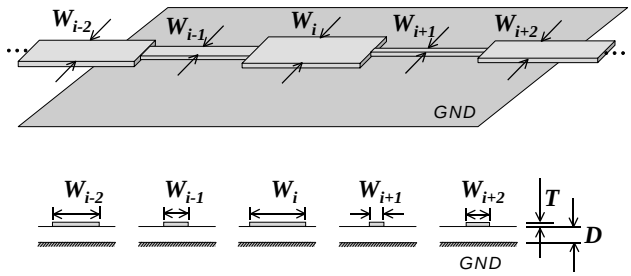


Fig. 2 Segmental Transmission Line (STL).



$$Z = f(W, T, D) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \frac{5.98D}{0.8W + T}$$

Fig. 3 Structure of STL in PCB.

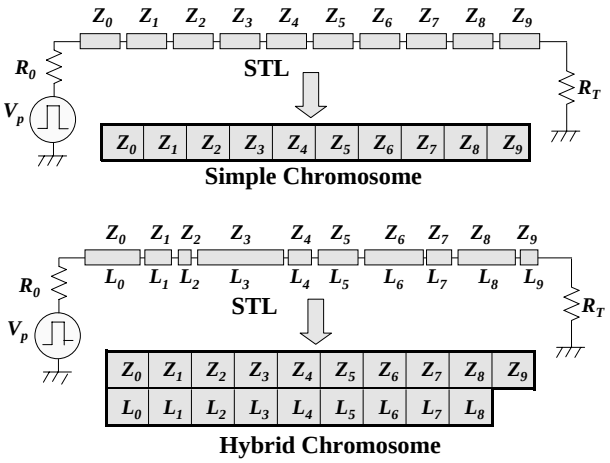


Fig. 4 Mapping of STL onto Chromosome

3. Genetic Algorithm for STL Design

We use the Minimal Generation Gap (MGG) algorithm, which is one of well-known genetic algorithms and was proposed to prevent the population from being occupied with the same kind of chromosomes and losing its diversity. In the MGG, a family is made from randomly selected parents in the *N*-th generation and their children generated by crossover operation as shown in Fig. 5. And one individual is selected from the family based on the elite or roulette selection and it is exchanged with one individual in the *N*-th generation to produce the *N*+1 generation. Since the waveform is very sensitive to the characteristic-impedance and segment-length in the STL, diversity of the population in the STL decreases frequently in its evolution. We thus use the MGG to avoid diversity-degradation in the evolutional STL design.

We use a fitness shown in Fig. 6. The difference area *Diff* between the ideal waveform *I*(t) and the current waveform *R*(t) is used for the fitness. The fitness is defined as the reciprocal of this difference area *Diff*.

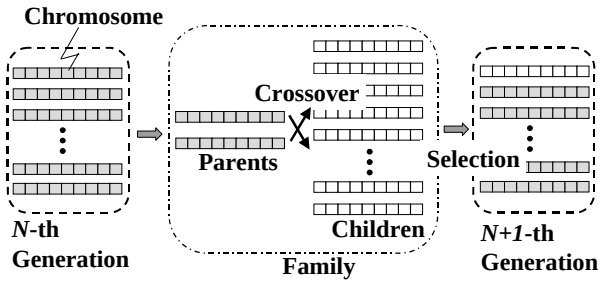
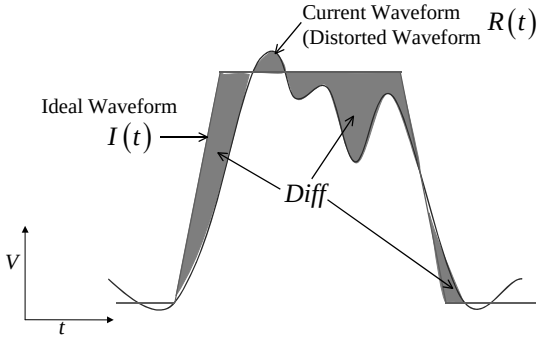


Fig. 5 MGG for STL Design.



$$Diff = \int_{-\frac{T}{2}}^{\frac{T}{2}} |I(t) - R(t)| dt \qquad fitness = \frac{1}{Diff}$$

Fig. 6 Fitness function in STL Design.

3. 250MHz STL Scale-up Prototype

3.1. Model and Design

We have developed a 250MHz scale-up prototype targeting a 1GHz memory-bus clock-distribution system shown in Fig. 6. One memory module (DIMM: Dual in-line Memory Module) is connected to a PCB trace, or transmission line. A clock-driver-LSI connected to the one end of the transmission line outputs a clock signal of 1GHz. The clock-signal propagates in the line of 15cm long and is distributed into the DIMM at two inputs connected to the line. Each input is equivalent to a load capacitance of 4pF, which causes the characteristic-impedance mismatch resulting the waveform distortion.

The 250MHz STL scale-up prototype is designed based on the 1GH DIMM: The transmission line length L and the load capacitance C_L are designed to 60cm and 15pF, respectively from the scale-up ratio of 4, i.e., 250MHz to 1GHz. And the transmission line of 60cm is divided into 15 segments (T1 to T15), totally. P_O in the figure is the first input from the clock-driver-LSI to the DIMM and it is the waveform-observation-point in this paper.

Table 1 shows the design result of characteristic impedance Z and length L of each segment (T1 to T15). We used a set of character impedances from 30Ω to 120Ω at 5Ω intervals in the MGG programs. As shown in the table, low-characteristic-impedance segments of 30 to 65 Ω and high-characteristic-impedance segments of 85 to 115 are assigned alternately. This means many reflection waves are generated in each boundary between adjacent segments, and they are used to improve the distorted wave.

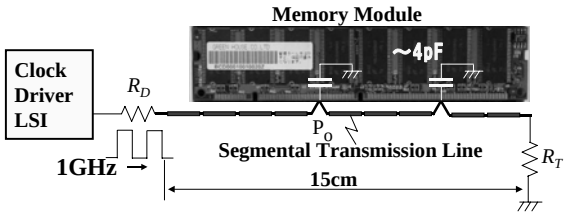


Fig. 6 1GHz DIMM Model.

Tab. 1 Design Result of 250MHz STL Scale-up Prototype.

Seg.	T1	T2	T3	T4	T5	T6	T7	T8
Z(Ω)	50	100	65	35	85	30	115	35
L(mm)	36.5	38.5	36.5	38.5	43.5	49.5	43	41.5
Seg.	T9	T10	T11	T12	T13	T14	T15	
Z(Ω)	90	30	110	65	40	85	90	
L(mm)	42	42.5	43	45	32.5	33	34.5	

3.2. Prototyping and Its Evaluation

We have fabricated a 250MHz STL scale-up prototype based on the design result shown in Tab. 1. The lower photograph in Fig. 7 is the STL prototype while the upper one is the conventional-transmission-line of Z =50Ω uniformly. In the figure of STL prototype, a part of the STL is magnified and shown also with values of the characteristic-impedance and the segment-length.

The STL and the conventional-transmission-line both run in each board of 31cm long in U-turn way, where the line-space is designed widely enough to avoid cross-talk noises. Two chip-capacitors (C_L) of 15pF each are connected to the line, which represent the input-capacitances of the memory module (DIMM). In the waveform observation, we used a digital-storage oscilloscope of 2GHz bandwidth and 10GS/s sampling-rate (WR204Xi, LeCroy Ltd.).

The upper waveform in Fig. 8 was observed at P_O in the conventional-transmission-line. The waveform is terribly and alarmingly distorted in its shape and amplitude: each pulse loses its sharpness in its rise and fall curves and have small jagged reflections on it. In addition, its amplitude is reduced to 1.06V from 1,8V of original input clock signal. As a result, the clock-signal in the conventional transmission line shown in Fig. 8 cannot be used in the DIMM clock-signals.

The lower waveform in Fig. 8 was observed at P_O in the STL. The distorted waveform in the conventional transmission line is well improved in the STL successfully: the reduced amplitude is restored to 1.6V, and jagged reflection noises disappear. The waveform is almost like a trapezoidal wave in its shape, which is close to the original clock-signal. The signal in the STL is thus enough for the clock-signal in its shape.

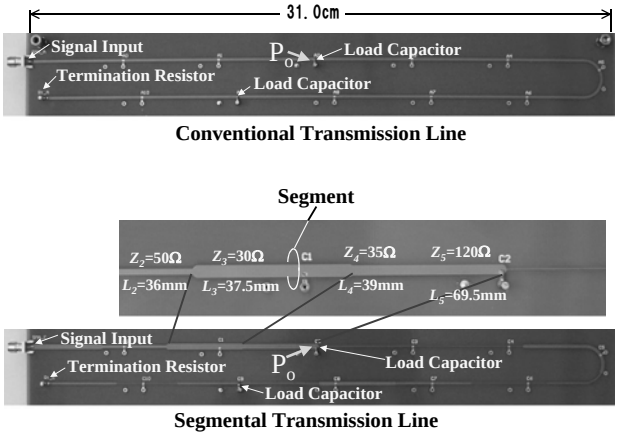


Fig. 7 Prototype Board: STL (lower) and Conventional Transmission Line (upper).

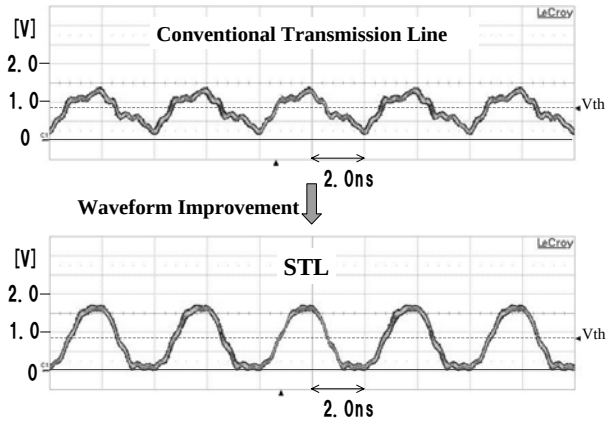


Fig. 8 Observed Clock Signals in Prototype.

3.3. Comparison with Simulations (Waveforms Designed Using GA)

Figures 9 and 10 show simulation results (upper) and observed waveforms (lower) in the conventional-transmission-line and STL, respectively. In the simulation results, the input-signal, which is sampled in the digital-sampling-oscilloscope and is used as the signal-source in the circuit simulator NGSPICE, is also shown synchronized with the distorted and improved waves, respectively.

In Fig. 9, the amplitude of the distorted signal in simulation is 1.23V, which is larger than the observed one in the prototype by 0.17V, but it is still smaller than the amplitude of the signal-source (1.8V). Even though the small jagged noises do not appear in the simulation, the waveforms in simulation and in the prototype almost resemble each other.

In Fig. 10, the improved signal in simulation matches the signal-source almost completely except the slight difference in its rising points. And the improved waveforms in the simulation and from the prototype observation well resemble each other. This means that the waveform well evolved taking after the source-signal.

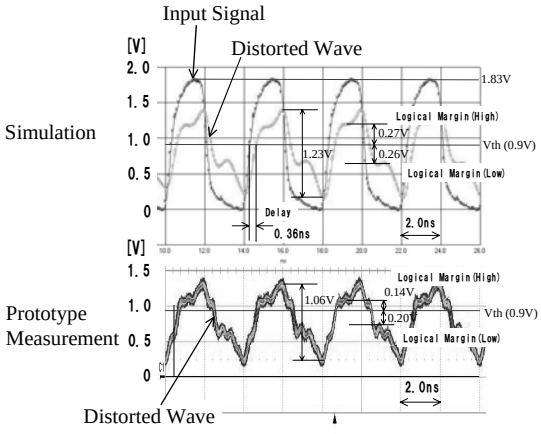


Fig. 9 Simulation results and Observed Waveform in Conventional Transmission Line.

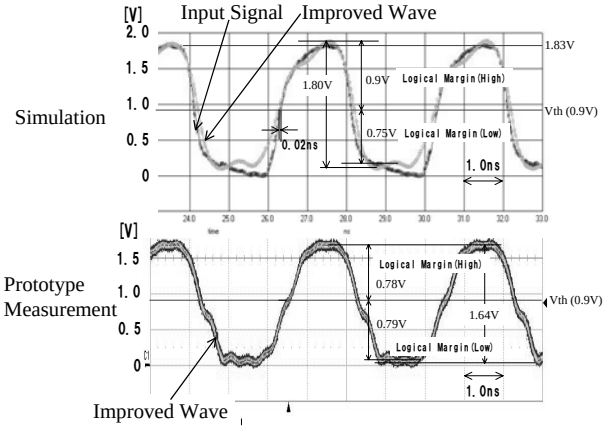


Fig. 10 Simulation results and Observed Waveform in STL.

4. Conclusions

A 250MHz scale-up STL (Segmental Transmission Line) to 1GHz DIMM (Dual In-line Memory Module) was designed using MGG (Minimum Generation Gap), which was one of well known genetic algorithms, and its prototype was fabricated. The observation result showed that the distorted waveform in the conventional transmission line was restored almost completely in the STL prototype. The observed waveform in the prototype was also well matched the design result, or the simulation result. Effectiveness of the STL to restore the distorted waveform and to ensure the SI (signal integrity) was thus well demonstrated experimentally using the prototype.

Acknowledgments

This work is partly supported by the 2010 cooperative research with The Semiconductor Technology Academic Research Center (STARC) in Japan.

References

[1] Moritoshi Yasunaga, Ikuo Yoshihara, and Jung, H. Kim, “The Design of Segmental-Transmission-Line for High-Speed Digital Signals Using Genetic Algorithms,” Proc. IEEE Congress on Evolutionary Computation (CEC) 2003, Vol. 3. pp. 1748-1755, Canberra, Australia, 2003.

[2] Koizumi, N., Yoshihara, I., Yamamori, K., and Yasunaga,M.:"Enhancement of the Variable-Length-Transmission-Line design method for multi-point optimization", Proc. 2006 IEEE Congress on Evolutionary Computation (CEC2006), CD-ROM, Vancouver, 2006.

[3] Moritoshi Yasunaga, Yoshiki Yamaguchi, Hiroshi Nakayama, Ikuo Yoshihara, Naoki Koizumi, and Jung H. Kim, “The Segmental-Transmission-Line: Its Design and Prototype Evaluation,” Proc. The 8th International Conference on Evolvable Systems, pp.130-140 Prague, Czech Republic, Sept. 2008.